Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic II

Chapter 7

Lec 7

FET Biasing

Prepared by

Asst Lecturer. Ahmed Saad Names

1. Introduction

The biasing levels for a silicon transistor configuration can be obtained using the approximate characteristic equations $VBE = 0.7$ V, $IC = \beta IB$, and $IC \approx IE$. The link between input and output variables is provided by b, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between *IC* and *IB*. Doubling the value of *IB* will double the level of *IC*, and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between *ID* and *VGS* can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have graphical solutions rather than mathematical solutions.

Another distinct difference between the analysis of BJT and FET transistors is that:

The controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.

In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0\,\text{A} \qquad (1)$$

$$I_D = I_S \qquad (2)$$

For JFETs and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (3)$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \qquad (4)$$

It is particularly important to realize that all of the equations above are for the field-effect transistor only! They do not change with each network configuration so long as the device is in the active region.

The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks.

2 Fixed-Bias Configuration

The simplest of biasing arrangements for the n-channel JFET appears in Fig. 1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach. Both methods are included in this section to demonstrate the difference between the two methods and also to establish the fact that the same solution can be obtained using either approach.

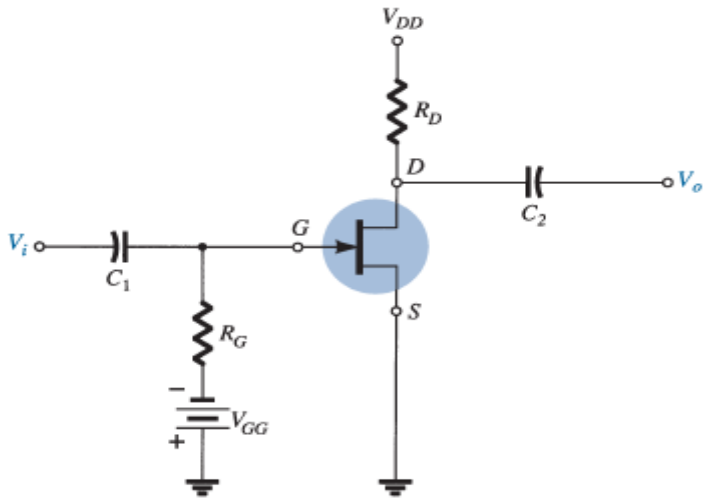


FIG. 1
Fixed-bias configuration.

The configuration of Fig. 1 includes the ac levels Vi and Vo and the coupling capacitors (C1 and C2). Recall that the coupling capacitors are “open circuits” for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor RG is present to ensure that Vi appears at the input to the FET amplifier for the ac analysis. For the dc analysis,

$$I_G \cong 0\,\text{A}$$
$$V_{R_G} = I_G R_G = (0\,\text{A})R_G = 0\,\text{V}$$

The zero-volt drop across RG permits replacing RG by a short-circuit equivalent, as appearing in the network of Fig. 2, specifically redrawn for the dc analysis. The fact that the negative terminal of the battery is connected directly to the defined positive potential of VGS clearly reveals that the polarity of VGS is directly opposite to that of VGG. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 2 results in

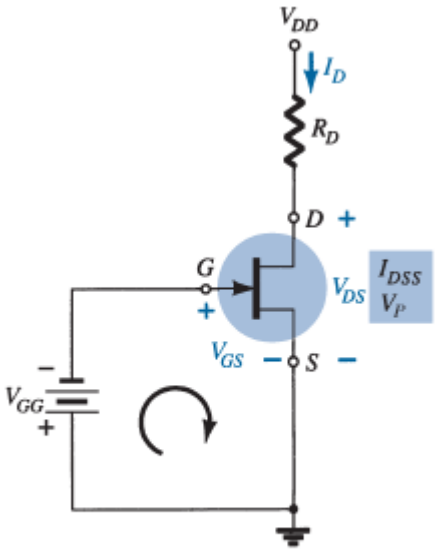


FIG. 2
Network for dc analysis.

$$-V_{GG} - V_{GS} = 0$$
$$\boxed{V_{GS} = -V_{GG}} \qquad (5)$$

Since VGG is a fixed dc supply, the voltage VGS is fixed in magnitude, resulting in the designation "fixed-bias configuration." The resulting level of drain current ID is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since *VGS* is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of *ID* calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct. A graphical analysis would require a plot of Shockley's equation as shown in Fig. 3. Recall that choosing *VGS* = *VP*/2 will result in a drain current of *IDSS*/4 when plotting the equation. For the analysis of this chapter, the three points defined by *IDSS*, *VP*, and the intersection just described will be sufficient for plotting the curve. In Fig. 4, the fixed level of *VGS* has been superimposed as a vertical line at *VGS* = -*VGG*. At any point on the vertical line, the level of *VGS* is -*VGG*—the level of *ID* must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point.*

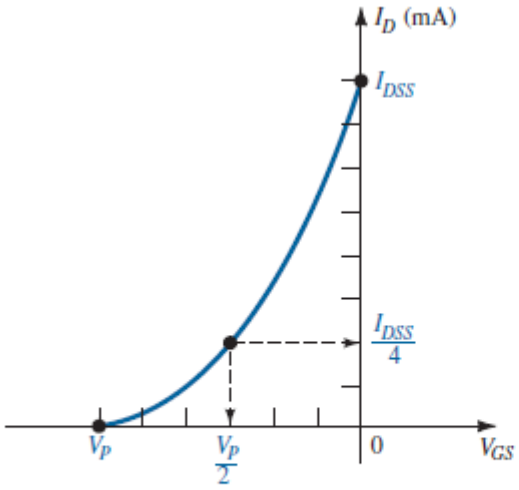


FIG. 3
Plotting Shockley's equation.

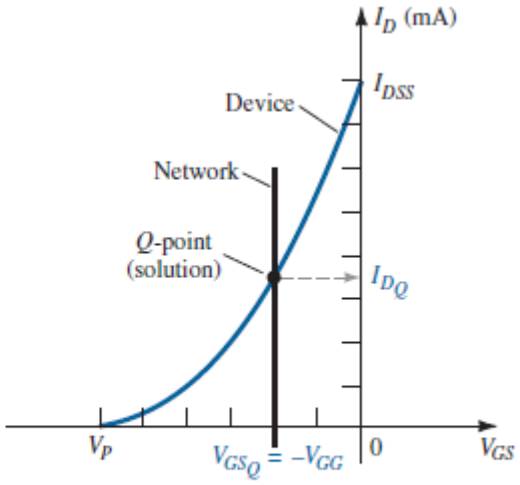


FIG. 4
Finding the solution for the fixed-bias configuration.

The subscript *Q* will be applied to the drain current and gate-to-source voltage to identify their levels at the *Q*-point. Note in Fig. 4 that the quiescent level of *ID* is determined by drawing a horizontal line from the *Q*-point to the vertical *ID* axis. It is important to realize that once the network of Fig. 1 is constructed and operating, the dc levels of ID and VGS that will be measured by the meters of Fig. 5 are the quiescent values defined by Fig. 4.

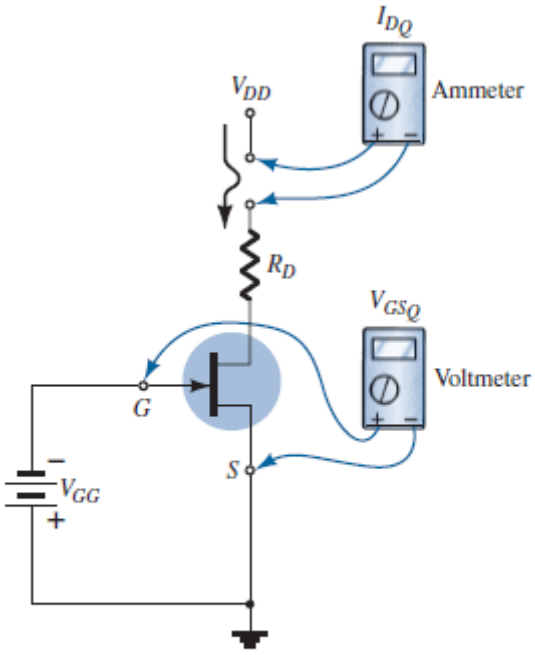


FIG. 5
Measuring the quiescent values of I_D and V_{GS}.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \qquad (6)$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 2,

$$\boxed{V_S = 0\ \text{V}} \qquad (7)$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$
$$V_D = V_{DS} + V_S = V_{DS} + 0\ \text{V}$$

$$\boxed{V_D = V_{DS}} \qquad (8)$$

$$V_{GS} = V_G - V_S$$
$$V_G = V_{GS} + V_S = V_{GS} + 0\ \text{V}$$

$$\boxed{V_G = V_{GS}} \qquad (9)$$

The fact that *VD* = *VDS* and *VG* = *VGS* is fairly obvious from the fact that *VS* = 0 V,

EXAMPLE 1 Determine the following for the network of Fig. 6:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

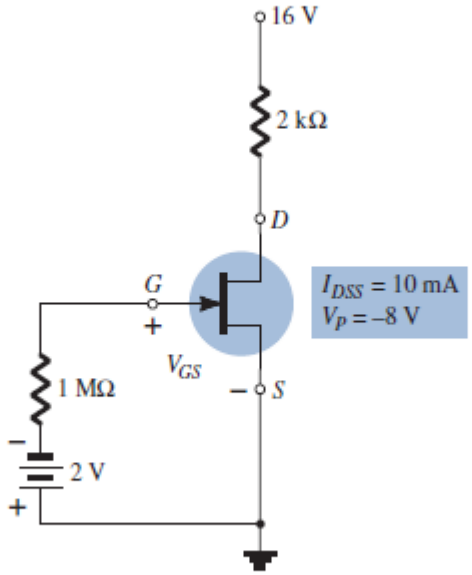


FIG. 6
Example 1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\ \text{mA}\left(1 - \frac{-2\ \text{V}}{-8\ \text{V}}\right)^2$
$= 10\ \text{mA}(1 - 0.25)^2 = 10\ \text{mA}(0.75)^2 = 10\ \text{mA}(0.5625)$
$= \mathbf{5.625\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.625\ \text{mA})(2\ \text{k}\Omega)$
$= 16\ \text{V} - 11.25\ \text{V} = \mathbf{4.75\ V}$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7. It is certainly difficult to read beyond the second place without

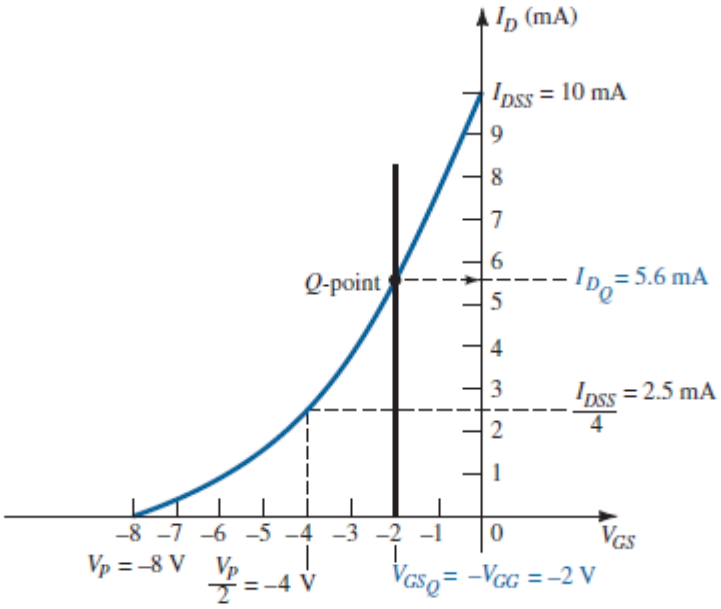


FIG. 7
Graphical solution for the network of Fig. 6.

significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7 is quite acceptable.

a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

b. $I_{D_Q} = \mathbf{5.6\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$
$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

d. $V_D = V_{DS} = \mathbf{4.8\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

3 Self-Bias Configuration

The self-bias configuration eliminates the need for two dc supplies. The controlling gate to- source voltage is now determined by the voltage across a resistor *RS* introduced in the source leg of the configuration as shown in Fig. 8.

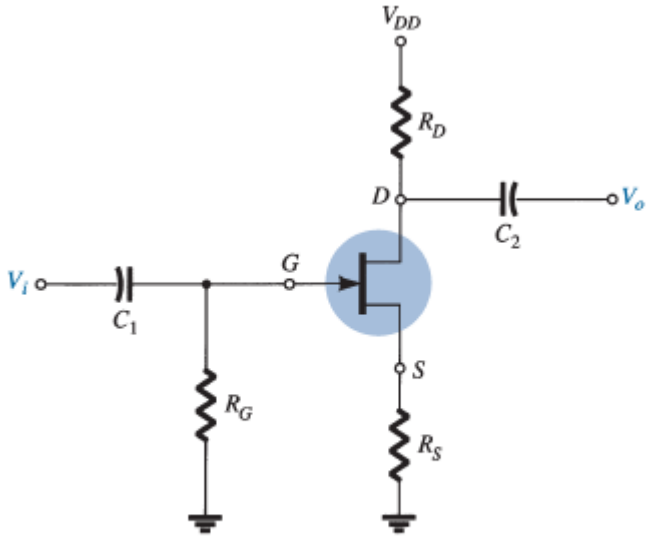


FIG. 8
JFET self-bias configuration.

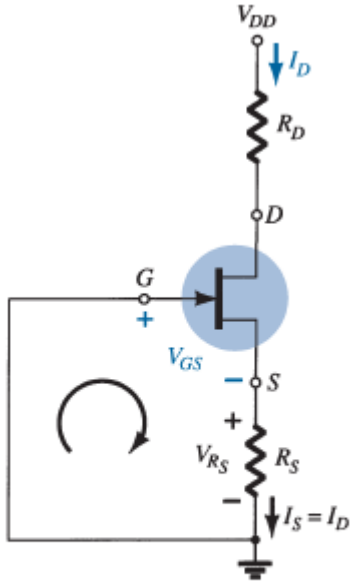


FIG. 9
DC analysis of the self-bias configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor *RG* replaced by a short-circuit equivalent since *IG* = 0 A. The result is the network of Fig. 9 for the important dc analysis. The current through *RS* is the source current *IS*, but *IS* = *ID* and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 9, we find that

$$-V_{GS} - V_{R_S} = 0$$

$$V_{GS} = -V_{R_S}$$

$$\boxed{V_{GS} = -I_D R_S} \qquad (10)$$

Note in this case that *VGS* is a function of the output current *ID* and not fixed in magnitude as occurred for the fixed-bias configuration. Equation (10) is defined by the network configuration, and Shockley's equation relates the input and output quantities of the device. Both equations relate the same two variables, *ID* and *VGS*, permitting either a mathematical or a graphical solution.

A mathematical solution could be obtained simply by substituting Eq. (10) into Shockley's equation as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$
$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, we obtain an equation of the following form

$$I_D = \frac{I_{DSS} \times R_S^2}{V_p^2}\left(I_D + \frac{V_P}{R_S}\right)^2 \rightarrow \frac{I_D \times V_p^2}{I_{DSS} \times R_S^2} = I_D^2 + 2I_D\frac{V_P}{R_S} + \frac{{V_P}^2}{{R_S}^2}$$

$$I_D^2 + I_D\left(2\frac{V_P}{R_S} - \frac{V_p^2}{I_{DSS} \times R_S^2}\right) + \frac{{V_P}^2}{{R_S}^2} = 0 \qquad \text{K1} = 2\frac{V_P}{R_S} - \frac{V_p^2}{I_{DSS} \times R_S^2}, \quad \text{K2} = \frac{{V_P}^2}{{R_S}^2}$$

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for ID. The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 10. Since Eq. (10) defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is ID = 0 A since it results in VGS = -ID RS = (0 A)RS = 0 V. For Eq. (10), therefore, one point on the straight line is defined by ID = 0 A and VGS = 0 V, as appearing on Fig. 10.

The second point for Eq. (10) requires that a level of VGS or ID be chosen and the corresponding level of the other quantity be determined using Eq. (10). The resulting levels of ID and VGS will then define another point on the

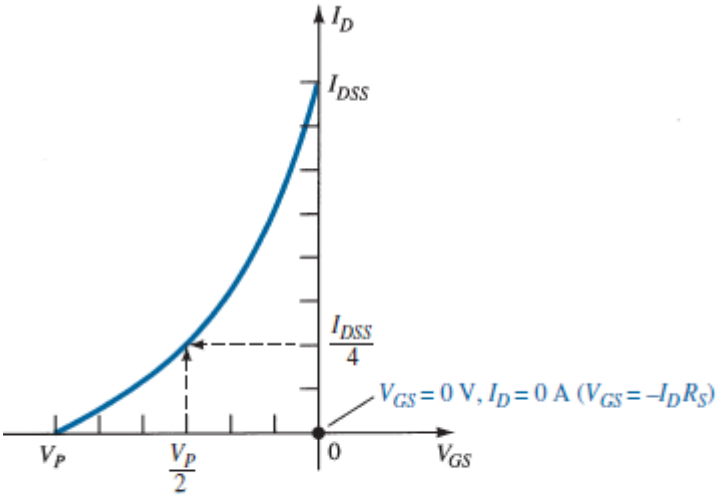


FIG. 10
Defining a point on the self-bias line.

straight line and permit the drawing of the straight line. Suppose, for example, that we choose a level of ID equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The result is a second point for the straight-line plot as shown in Fig. 11. The straight line as defined by Eq. (10) is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve.

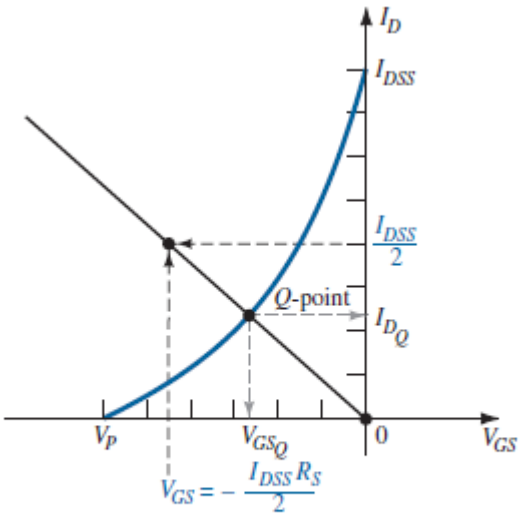


FIG. 11
Sketching the self-bias line.

The quiescent values of ID and VGS can then be determined and used to find the other quantities of interest. The level of VDS can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but $$I_D = I_S$$

and

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \qquad (11)$$

In addition,

$$\boxed{V_S = I_D R_S} \qquad (12)$$

$$\boxed{V_G = 0\,\text{V}} \qquad (13)$$

and

$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}} \qquad (14)$$

EXAMPLE 2 Determine the following for the network of Fig. 12:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

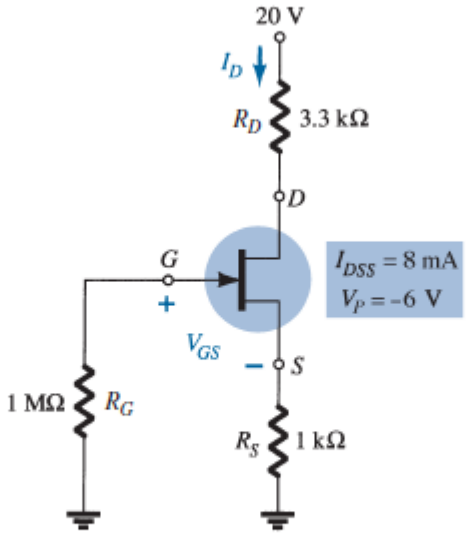


FIG. 12
Example 2.

Solution:

a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

$$V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$$

The result is the plot of Fig. 13 as defined by the network.

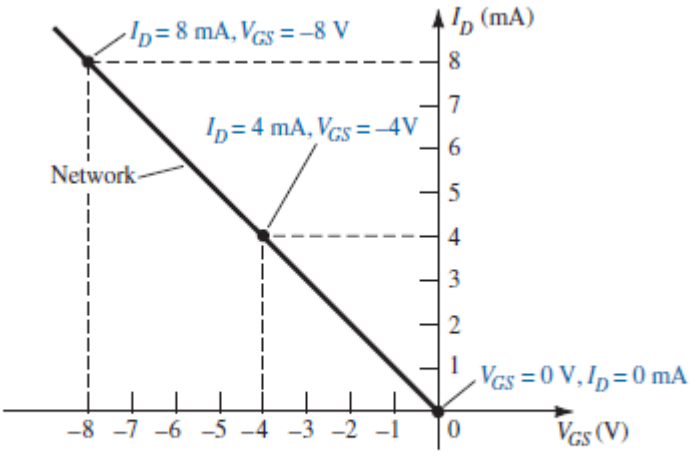


FIG. 13
Sketching the self-bias line for the network of Fig. 12.

If we happen to choose ID = 8 mA, the resulting value of VGS would be -8 V, as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of ID can be chosen as long as the corresponding value of VGS

as determined by Eq. (10) is employed. In addition, keep in mind that the value of VGS could be chosen and the value of ID determined graphically. For Shockley's equation, if we choose VGS = VP/2 = -3 V, we find that ID = IDSS/4 = 8 mA/4 = 2 mA, and the plot of Fig. 14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 13 on the device characteristics of Fig. 14 and finding the point of intersection of the two as indicated on Fig. 15. The resulting operating point results in a quiescent value of gate-to-source voltage of VGSQ = -2.6 V

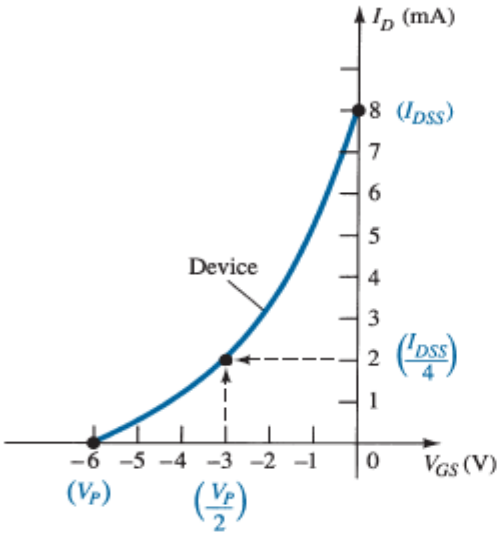


FIG. 14
Sketching the device characteristics for the JFET of Fig. 12.

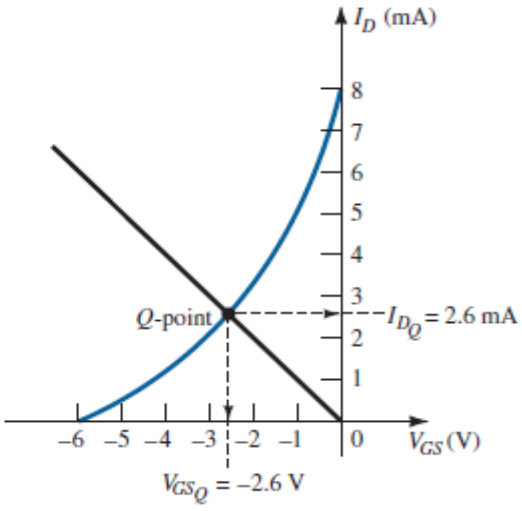


FIG. 15
Determining the Q-point for the network of Fig. 12.

b. At the quiescent point

$$I_{D_Q} = \mathbf{2.6\ mA}$$

c. Eq. (11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}\Omega)$
$= 20\ \text{V} - 11.18\ \text{V}$
$= \mathbf{8.82\ V}$

d. Eq. (12): $V_S = I_D R_S$
$= (2.6\ \text{mA})(1\ \text{k}\Omega)$
$= \mathbf{2.6\ V}$

e. Eq. (13): $V_G = \mathbf{0\ V}$

f. Eq. (14): $V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$

or $V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

EXAMPLE 3 Find the quiescent point for the network of Fig. 12 if:

a. $R_S = 100\ \Omega$.
b. $R_S = 10\ \text{k}\Omega$.

Solution: Both $R_S = 100\ \Omega$ and $R_S = 10\ \text{k}\Omega$ are plotted on Fig. 16.

a. For $R_S = 100\ \Omega$:

$$I_{D_Q} \cong \mathbf{6.4\ mA}$$

and from Eq. (10),

$$V_{GS_Q} \cong \mathbf{-0.64\ V}$$

b. For $R_S = 10\ \text{k}\Omega$

$$V_{GS_Q} \cong \mathbf{-4.6\ V}$$

and from Eq. (10),

$$I_{D_Q} \cong \mathbf{0.46\ mA}$$

In particular, note how lower levels of RS bring the load line of the network closer to the ID axis, whereas increasing levels of RS bring the load line closer to the VGS axis.

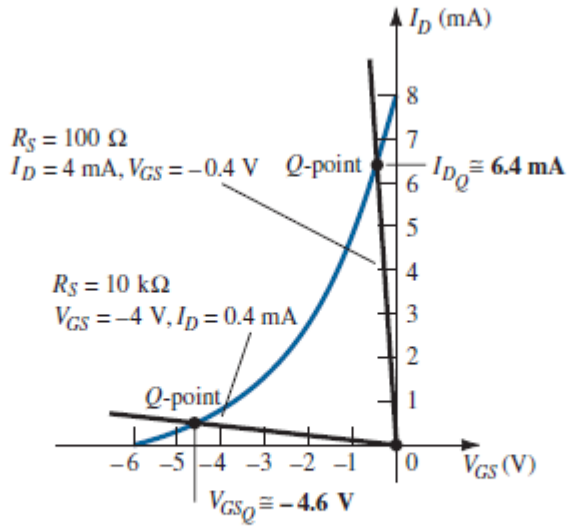


FIG. 16
Example 3.

4 Voltage-Divider Biasing

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 17. The basic construction is exactly the same, but the dc analysis of each is quite different. *IG* = 0 A for FET amplifiers, but the magnitude of *IB* for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that *IB* provides the link between input and output circuits for the BJT voltage-divider configuration, whereas *VGS* does the same for the FET configuration.

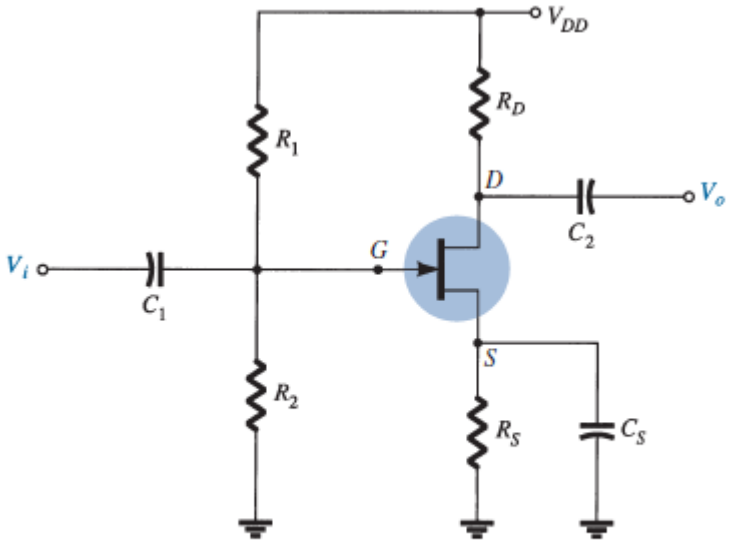


FIG. 17
Voltage-divider bias arrangement.

The network of Fig. 17 is redrawn as shown in Fig. 18 for the dc analysis. Note that all the capacitors, including the bypass capacitor *CS*, have been replaced by an "open-circuit" equivalent in Fig. 18b. In addition, the source *VDD* was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since *IG* = 0 A, Kirchhoff's current law requires that *IR*1 = *IR*2, and the series equivalent circuit appearing to the left of the figure can be used to find the level of *VG*. The voltage *VG*, equal to the voltage across *R*2, can be found using the voltage-divider rule and Fig. 18a as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad (15)$$

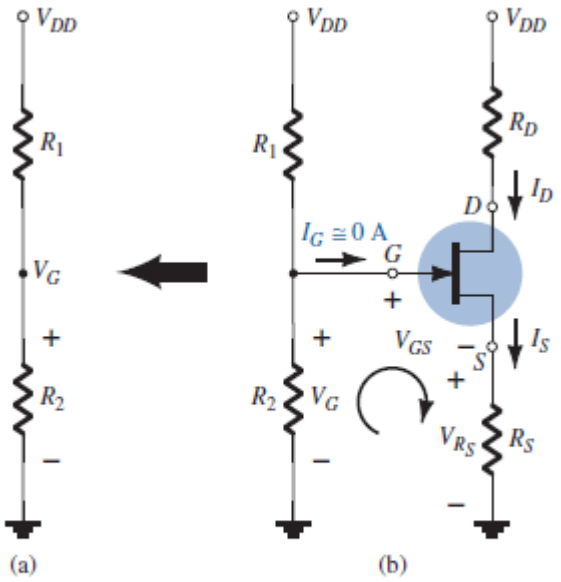


FIG. 18
Redrawn network of Fig. 17 for dc analysis.

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 18 results in

$$V_G - V_{GS} - V_{R_S} = 0$$
$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$\boxed{V_{GS} = V_G - I_D R_S} \qquad (16)$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: VGS and ID. The quantities VG and RS are fixed by the network construction. Equation (16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. 19 the current ID = 0 mA. If we therefore select ID to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting ID = 0 mA into Eq. (16) and finding the resulting value of VGS as follows:

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\text{ mA})R_S$$

$$\boxed{V_{GS} = V_G|_{I_D=0\text{ mA}}} \qquad (17)$$

The result specifies that whenever we plot Eq. (16), if we choose ID = 0 mA, the value of VGS for the plot will be VG volts. The point just determined appears in Fig. 19.

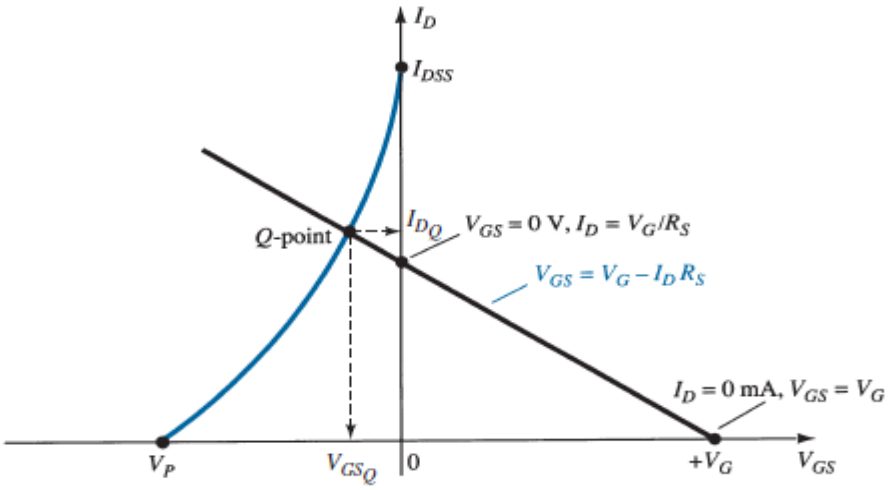


FIG. 19
Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis *VGS* = 0 V and solve for the resulting value of *ID*:

$$V_{GS} = V_G - I_D R_S$$
$$0\text{ V} = V_G - I_D R_S$$

$$\boxed{I_D = \frac{V_G}{R_S}\bigg|_{V_{GS}=0\text{ V}}} \qquad (18)$$

The result specifies that whenever we plot Eq. (16), if VGS = 0 V, the level of ID is determined by Eq. (18). This intersection also appears on Fig. 19. The two points defined above permit the drawing of a straight line to represent Eq. (16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of ID and VGS. Since the intersection on the vertical axis is determined by ID = VG>RS and VG is fixed by the input network, increasing values of RS will reduce the level of the ID intersection as

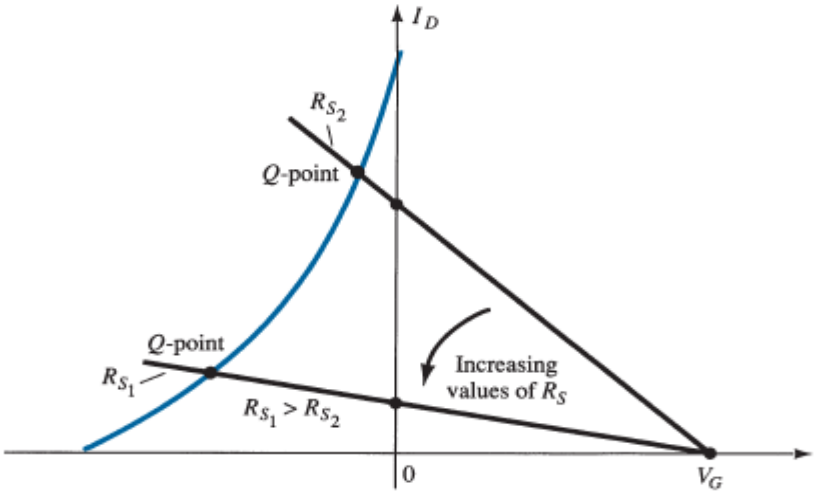


FIG. 20
Effect of R_S on the resulting Q-point.

shown in Fig. 20. It is fairly obvious from Fig. 20 that:

Increasing values of RS result in lower quiescent values of ID and declining values of VGS.

Once the quiescent values of IDQ and VGSQ are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \quad (19)$$

$$V_D = V_{DD} - I_D R_D \quad (20)$$

$$V_S = I_D R_S \quad (21)$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2} \quad (22)$$

EXAMPLE 4 Determine the following for the network of Fig. 21:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.

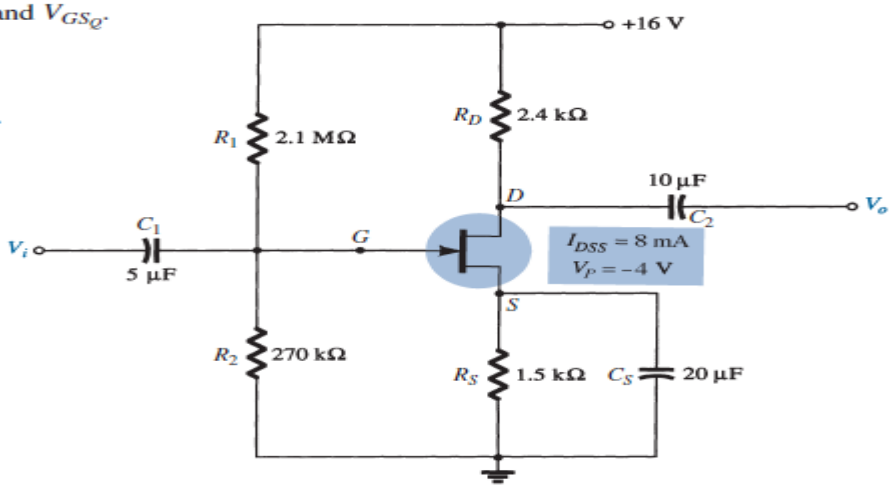


FIG. 21
Example 4.

Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\,\text{mA}/4 = 2\,\text{mA}$, then $V_{GS} = V_P/2 = -4\,\text{V}/2 = -2\,\text{V}$. The resulting curve representing Shockley's equation appears in Fig. 22. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$
$$= \frac{(270\,\text{k}\Omega)(16\,\text{V})}{2.1\,\text{M}\Omega + 0.27\,\text{M}\Omega}$$
$$= 1.82\,\text{V}$$

and
$$V_{GS} = V_G - I_D R_S$$
$$= 1.82\,\text{V} - I_D(1.5\,\text{k}\Omega)$$

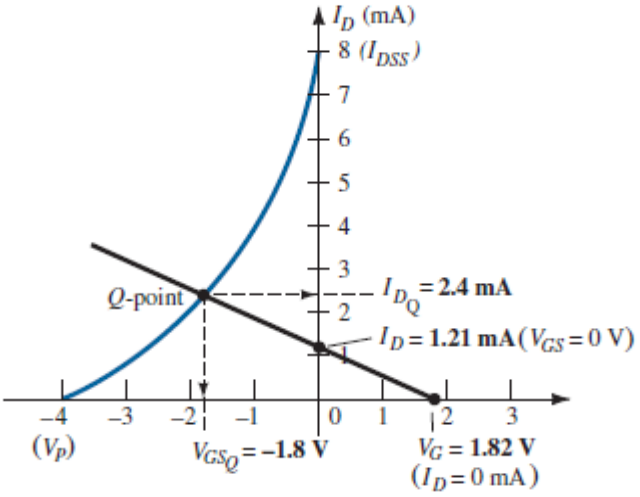


FIG. 22
Determining the Q-point for the network of Fig. 21.

When $I_D = 0\,\text{mA}$,

$$V_{GS} = +1.82\,\text{V}$$

When $V_{GS} = 0\,\text{V}$,

$$I_D = \frac{1.82\,\text{V}}{1.5\,\text{k}\Omega} = 1.21\,\text{mA}$$

The resulting bias line appears on Fig. 22 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\,mA}$$

and
$$V_{GS_Q} = \mathbf{-1.8\,V}$$

b. $V_D = V_{DD} - I_D R_D$
$= 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega)$
$= \mathbf{10.24\,V}$

c. $V_S = I_D R_S = (2.4\,\text{mA})(1.5\,\text{k}\Omega)$
$= \mathbf{3.6\,V}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega + 1.5\,\text{k}\Omega)$
$= \mathbf{6.64\,V}$

or $V_{DS} = V_D - V_S = 10.24\,\text{V} - 3.6\,\text{V}$
$= \mathbf{6.64\,V}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24\text{ V} - 1.82\text{ V}$$
$$= \mathbf{8.42\text{ V}}$$

5 Common-Gate Configuration

The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown in Fig. 23a. The network can also be drawn as shown in Fig. 23b.

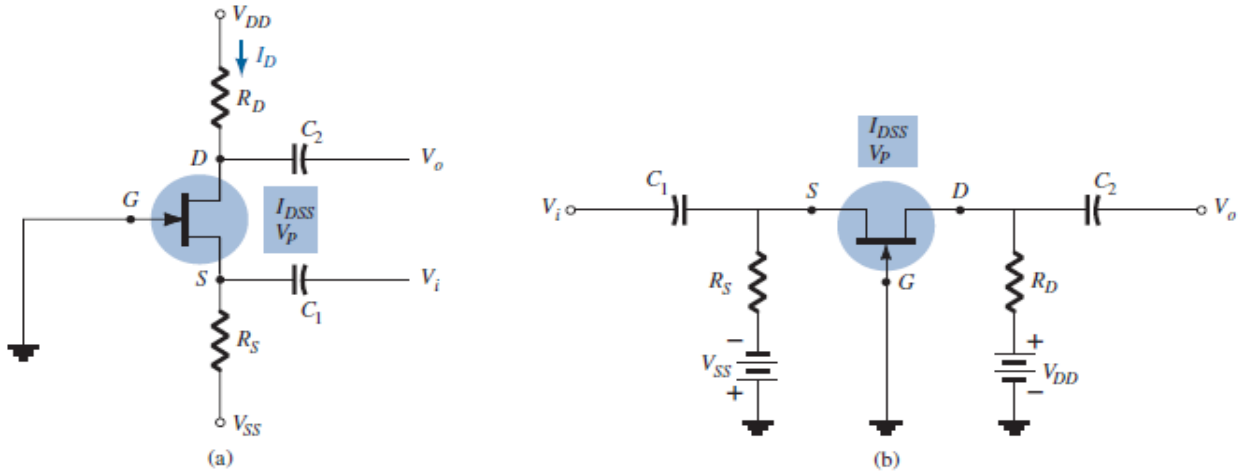


FIG. 23
Two versions of the common-gate configuration.

The network equation can be determined using Fig. 24. Applying Kirchhoff's voltage law in the direction shown in Fig. 24 will result in

$$-V_{GS} - I_S R_S + V_{SS} = 0$$
$$V_{GS} = V_{SS} - I_S R_S$$
$$I_S = I_D$$

$$\boxed{V_{GS} = V_{SS} - I_D R_S} \qquad \textbf{(23)}$$

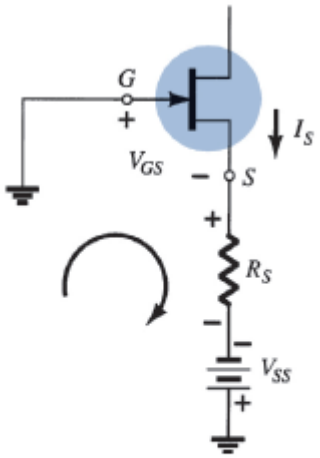


FIG. 24
Determining the network equation for the configuration of Fig. 23.

Applying the condition ID = 0 mA to Eq. 23 will result in

$$V_{GS} = V_{SS} - (0)R_S$$

$$\boxed{V_{GS} = V_{SS}|_{I_D=0\text{mA}}} \qquad \textbf{(24)}$$

Applying the condition *VGS* = 0 V to Eq. 23 will result in

$$0 = V_{SS} - I_D R_S$$

$$\boxed{I_D = \frac{V_{SS}}{R_S}\bigg|_{V_{GS}=0\text{ V}}} \qquad \textbf{(25)}$$

The resulting load-line appears in Fig. 25 intersecting the transfer curve for the JFET as shown in the figure. The resulting intersection defines the operating current *IDQ* and voltage *VDQ* for the network as also indicated in the network.

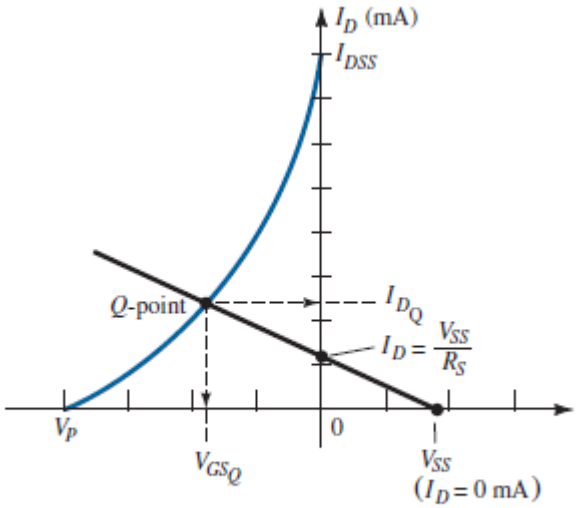


FIG. 25
Determining the Q-point for the network of Fig. 24.

Applying Kirchhoff's voltage law around the loop containing the two sources, the JFET and the resistors RD and RS in Fig. 23a and Fig. 23b will result in

$$+V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

Substituting $I_S = I_D$ we have

$$+V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$$

so that $$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)} \quad (26)$$

with $$\boxed{V_D = V_{DD} - I_D R_D} \quad (27)$$

and $$\boxed{V_S = -V_{SS} + I_D R_S} \quad (28)$$

EXAMPLE 5 Determine the following for the common-gate configuration of Fig. 26:

a. V_{GS_Q}
b. I_{D_Q}
c. V_D
d. V_G
e. V_S
f. V_{DS}

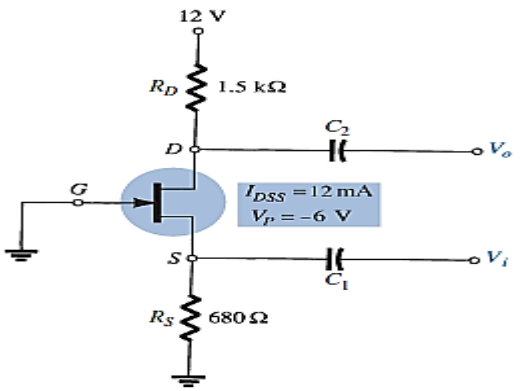


FIG. 26
Example 5.

Solution: Even though *VSS* is not present in this common-gate configuration the equations derived above can still be used by simply substituting *VSS* = 0 V into each equation in which it appears.

a. For the transfer characteristics Eq. 23 becomes

$$V_{GS} = 0 - I_D R_S$$
$$V_{GS} = -I_D R_S$$

For this equation the origin is one point on the load line while the other must be determined at some arbitrary point. Choosing *ID* = 6 mA and solving for *VGS* will result in the following:

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

as shown in Fig. 27.

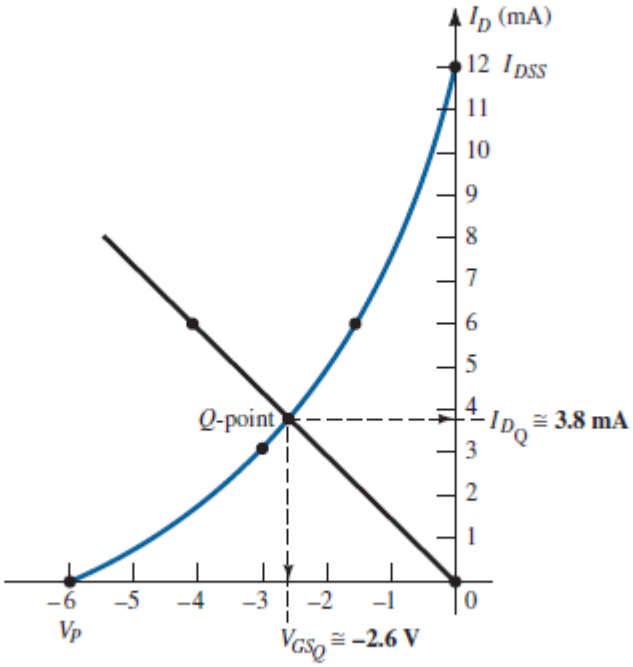


FIG. 27
Determining the Q-point for the network of Fig. 26.

The device transfer curve is sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}(\text{at } V_P/2)$$

and $$V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = -1.8\text{ V}\ (\text{at } I_D = I_{DSS}/2)$$

The resulting solution is:

$$V_{GS_Q} \cong \mathbf{-2.6\text{ V}}$$

b. From Fig. 27,

$$I_{D_Q} \cong \mathbf{3.8\text{ mA}}$$

c. $V_D = V_{DD} - I_D R_D$
$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$
$= \mathbf{6.3\text{ V}}$

d. $V_G = \mathbf{0\text{ V}}$

e. $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$
$= \mathbf{2.58\text{ V}}$

f. $V_{DS} = V_D - V_S$
$= 6.3\text{ V} - 2.58\text{ V}$
$= \mathbf{3.72\text{ V}}$

6 Special Case: *VGS Q* = 0 V

A network of recurring practical value because of its relative simplicity is the configuration of Fig. 28. Note that direct connection of the gate and source terminals to ground resulting in *VGS* = 0 V. It specifies that for any dc condition the gate to source voltage must be zero volts. This will result in a vertical load line at *VGSQ* = 0 V as shown in Fig. 29.

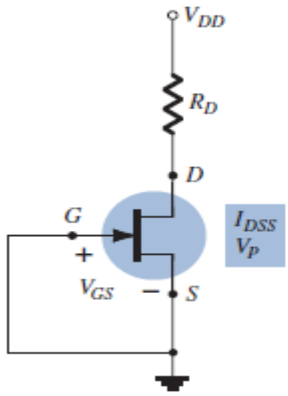


FIG. 28
Special case $V_{GS_Q} = 0$ V configuration.

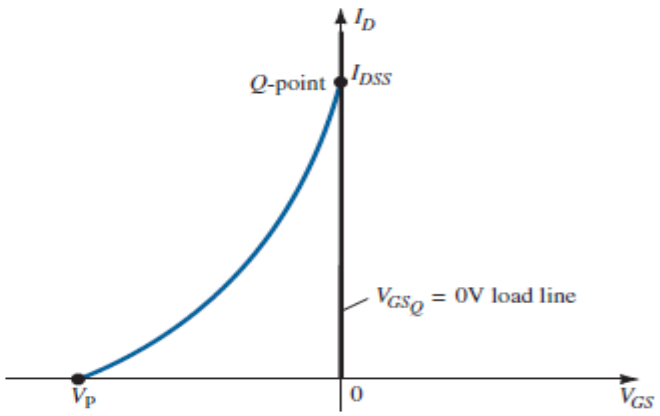


FIG. 29
Finding the Q-point for the network of Fig. 28.

Since the transfer curve of a JFET will cross the vertical axis at *IDSS* the drain current for the network is set at that level.

Therefore, $\boxed{I_{D_Q} = I_{DSS}}$ **(29)**

Applying Kirchhoff's voltage law:

$$V_{DD} - I_D R_D - V_{DS} = 0$$

and $\boxed{V_{DS} = V_{DD} - I_D R_D}$ **(30)**

with $\boxed{V_D = V_{DS}}$ **(31)**

and $\boxed{V_S = 0\text{ V}}$ **(32)**

7 Depletion-Type MOSFETS

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of *VGS* and levels of *ID* that exceed *IDSS*. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of *VGS*. How far into the region of positive values of *VGS* and values of *ID* greater than *IDSS* does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the effect of the change in device on the resulting analysis.

EXAMPLE 6 For the *n*-channel depletion-type MOSFET of Fig. 30, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.

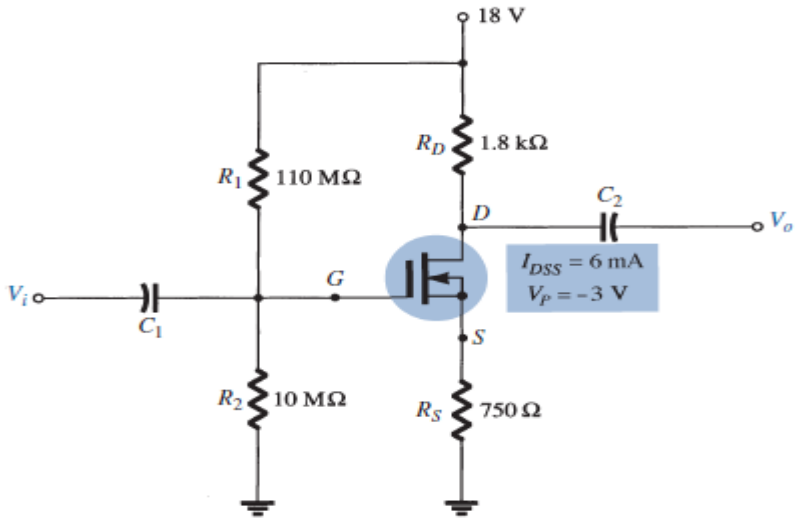


FIG. 30
Example 6.

Solution:

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778)$$
$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 31. Proceeding as described for JFETs, we have

$$\text{Eq. (15):}\quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$
$$\text{Eq. (16):}\quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

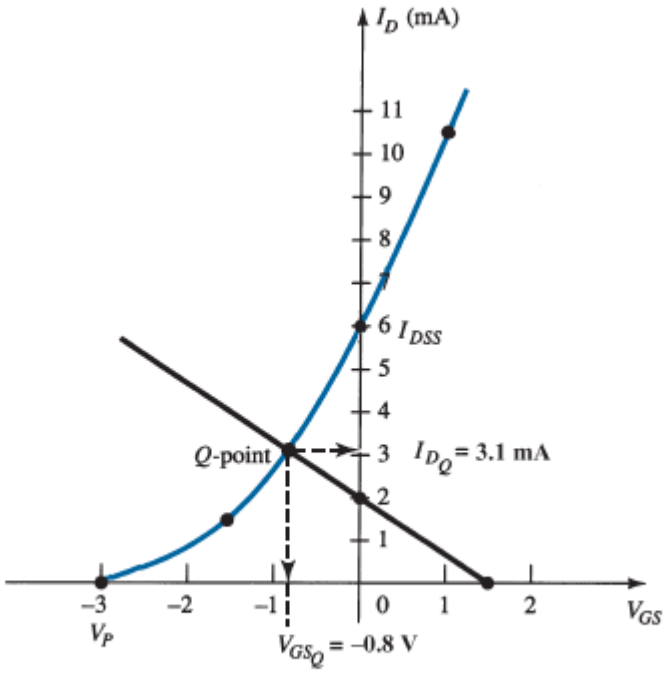


FIG. 31
Determining the Q-point for the network of Fig. 30.

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 31. The resulting operating point is given by

$$I_{D_Q} = \mathbf{3.1\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-0.8\text{ V}}$$

b. Eq. (19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$$
$$\cong \mathbf{10.1\text{ V}}$$

EXAMPLE 7 Repeat Example 6 with $R_S = 150\ \Omega$.

Solution:

a. The plot points are the same for the transfer curve as shown in Fig. 32. For the bias line,

$$V_{GS} = V_G - I_D R_S = 1.5\ \text{V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5\ \text{V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\ \text{V}}{150\ \Omega} = 10\ \text{mA}$$

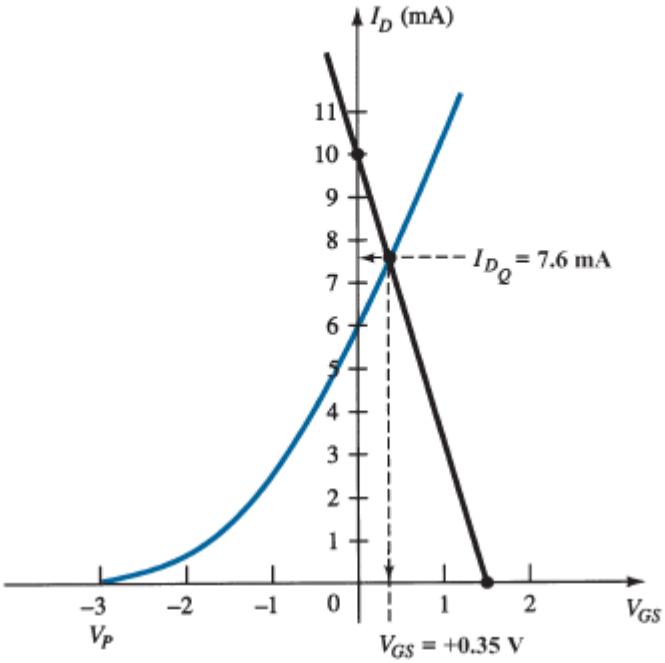


FIG. 32
Example 7.

The bias line is included on Fig. 32. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result is

$$I_{D_Q} = \mathbf{7.6\ mA}$$
$$V_{GS_Q} = \mathbf{+0.35\ V}$$

b. Eq. (19):

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 18\ \text{V} - (7.6\ \text{mA})(1.8\ \text{k}\Omega + 150\ \Omega) \\ &= \mathbf{3.18\ V} \end{aligned}$$

EXAMPLE 8 Determine the following for the network of Fig. 33:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.

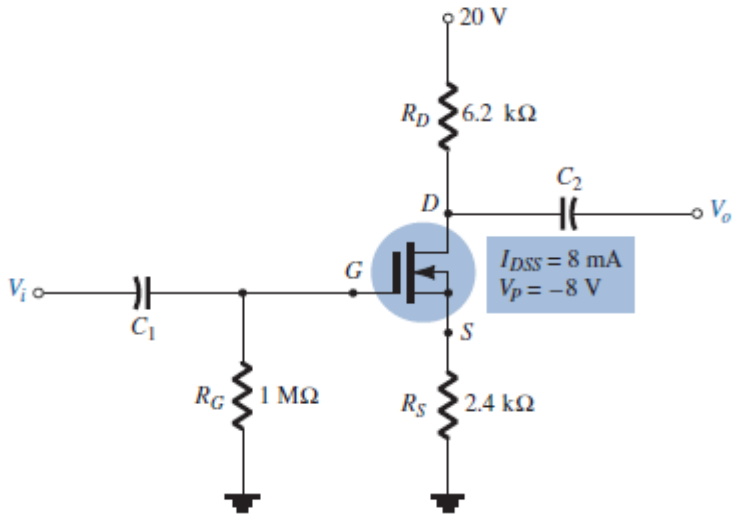


FIG. 33
Example 8.

Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\text{ mA}}{4} = 2\text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8\text{ V}}{2} = -4\text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2\text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{+2\text{ V}}{-8\text{ V}}\right)^2$$

$$= 12.5\text{ mA}$$

The resulting transfer curve appears in Fig. 34. For the network bias line, at $V_{GS} = 0$ V, $I_D = 0$ mA. Choosing $V_{GS} = -6$ V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point is given by

$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$
$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$
$= \mathbf{9.46\text{ V}}$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

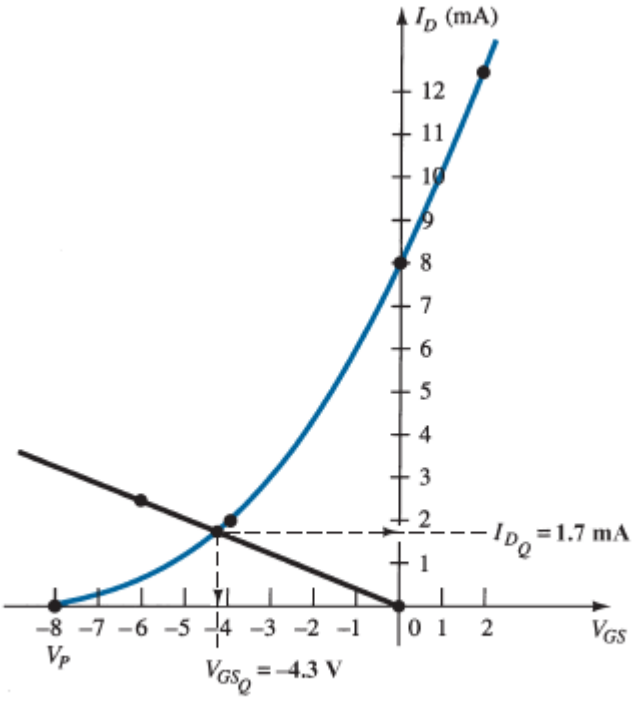


FIG. 34
Determining the Q-point for the network of Fig. 33.

EXAMPLE 9 Determine V_{DS} for the network of Fig. 35.

Solution: The direct connection between the gate and source terminals requires that

$$V_{GS} = 0 \text{ V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS_Q} = \mathbf{0 \text{ V}}$$

and

$$I_{D_Q} = \mathbf{10 \text{ mA}}$$

There is therefore no need to draw the transfer curve, and

$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (10 \text{ mA})(1.5 \text{ k}\Omega)$$
$$= 20 \text{ V} - 15 \text{ V}$$
$$= \mathbf{5 \text{ V}}$$

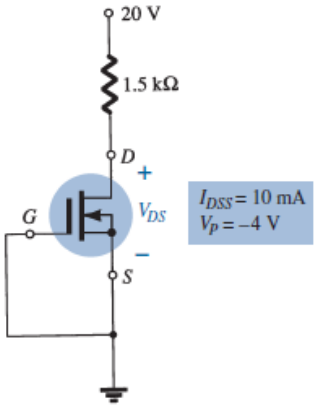


FIG. 35
Example 9.

8 Enhancement-Type MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate to- source voltage less than the threshold level *VGS*(Th), as shown in Fig. 36. For levels of *VGS* greater than *VGS*(Th), the drain current is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2 \qquad (33)$$

Since specification sheets typically provide the threshold voltage and a level of drain current (ID(on)) and its corresponding level of VGS(on), two points are defined immediately as shown in Fig. 36. To complete the curve, the constant k of Eq. (33) must be determined from the specification sheet data by substituting into Eq. (33) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$
$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

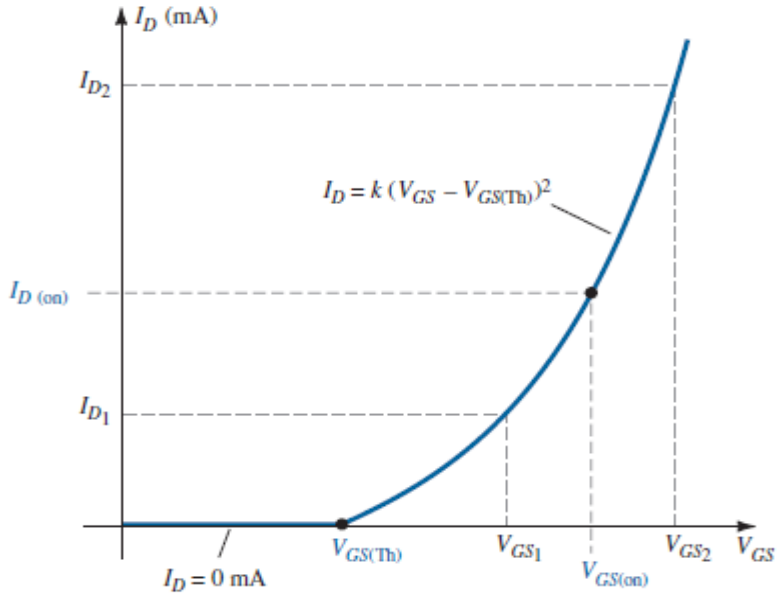


FIG. 36
Transfer characteristics of an n-channel enhancement-type MOSFET.

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \qquad (34)$$

Once k is defined, other levels of ID can be determined for chosen values of VGS. Typically, a point between VGS(Th) and VGS(on) and one just greater than VGS(on) will provide a sufficient number of points to plot Eq. (33) (note ID1 and ID2 on Fig. 36).

8.1 Feedback biasing arrangement

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 37. The resistor RG brings a suitably large voltage to the gate to drive the MOSFET "on." Since IG = 0 mA, VRG = 0 V and the dc equivalent network appears as shown in Fig. 38.

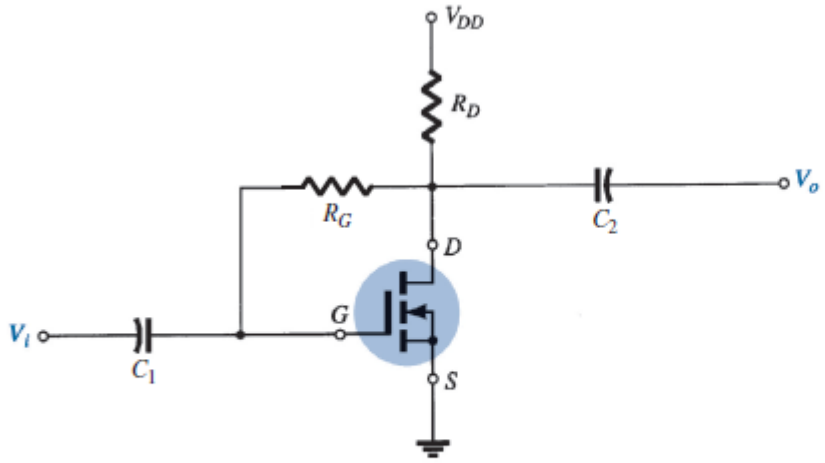


FIG. 37
Feedback biasing arrangement.

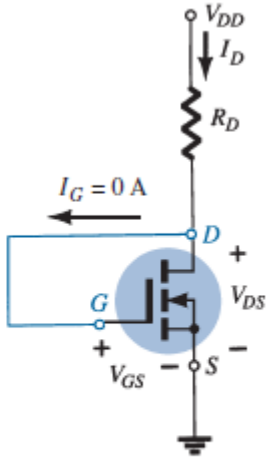


FIG. 38
DC equivalent of the network of Fig. 37.

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$\boxed{V_{DS} = V_{GS}} \qquad (35)$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (27):

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \qquad (36)$$

The result is an equation that relates ID to VGS, permitting the plot of both on the same set of axes. Since Eq. (36) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting ID = 0 mA into Eq. (36) gives

$$V_{GS} = V_{DD}|_{I_D=0\text{ mA}} \tag{37}$$

Substituting $V_{GS} = 0$ V into Eq. (36), we have

$$I_D = \left.\frac{V_{DD}}{R_D}\right|_{V_{GS}=0\text{ V}} \tag{38}$$

The plots defined by Eqs. (33) and (36) appear in Fig. 39 with the resulting operating point.

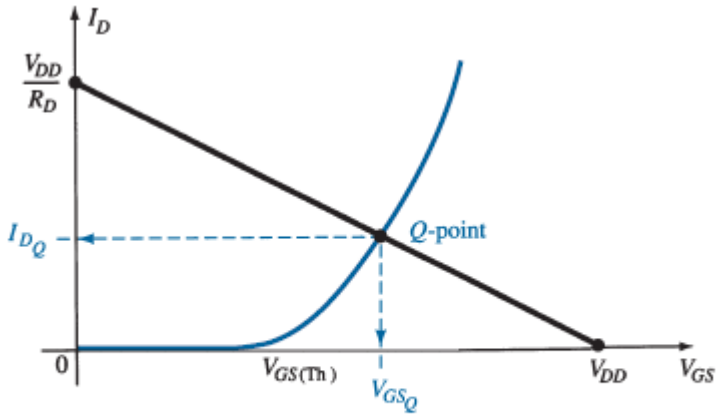


FIG. 39
Determining the Q-point for the network of Fig. 37.

EXAMPLE 10 Determine I_{D_Q} and V_{DS_Q} for the enhancement-type MOSFET of Fig. 40.

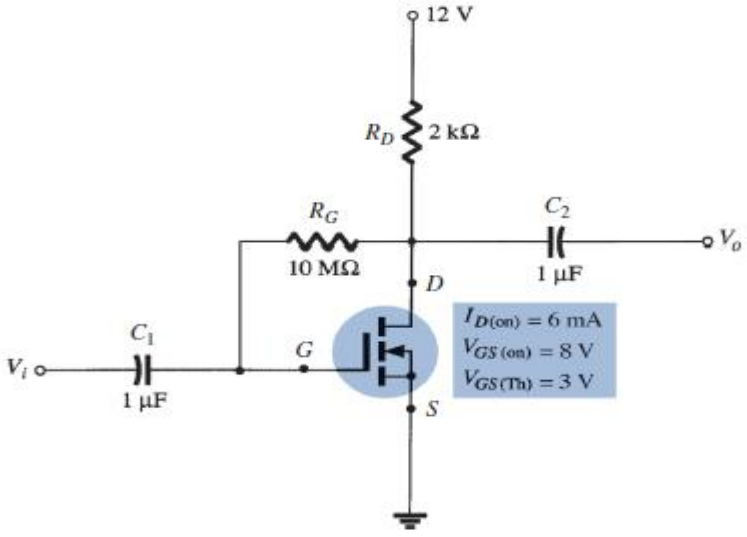


FIG. 40
Example 10.

Solution:

plotting the transfer Curve Two points are defined immediately as shown in Fig. 41.

Solving for k, we obtain

Eq. (34):
$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$
$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{A/V}^2$$
$$= \mathbf{0.24 \times 10^{-3}\text{ A/V}^2}$$

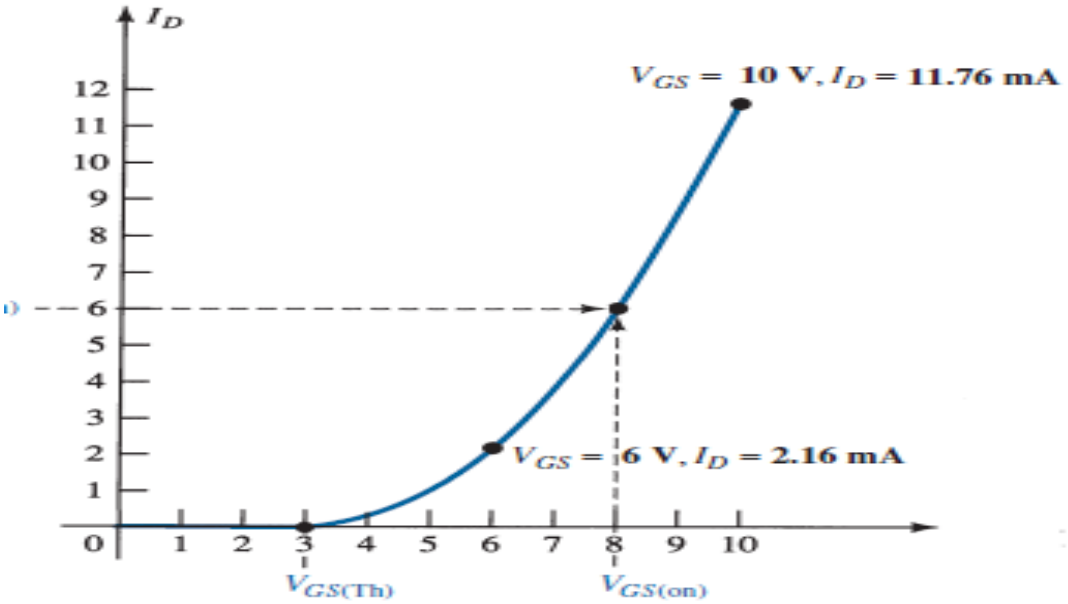


FIG. 41
Plotting the transfer curve for the MOSFET of Fig. 40.

For $V_{GS} = 6$ V (between 3 and 8 V):
$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$
$$= 2.16\text{ mA}$$
as shown on Fig. 41. For $V_{GS} = 10$ V (slightly greater than $V_{GS(Th)}$),
$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\text{ mA}$$
as also appearing on Fig. 41. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 41.

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$
Eq. (37): $$V_{GS} = V_{DD} = 12\text{ V}|_{I_D = 0\text{ mA}}$$
Eq. (38): $$I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}|_{V_{GS} = 0\text{ V}}$$

The resulting bias line appears in Fig. 42.

At the operating point,

$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$
and
$$V_{GS_Q} = 6.4\text{ V}$$
with
$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$

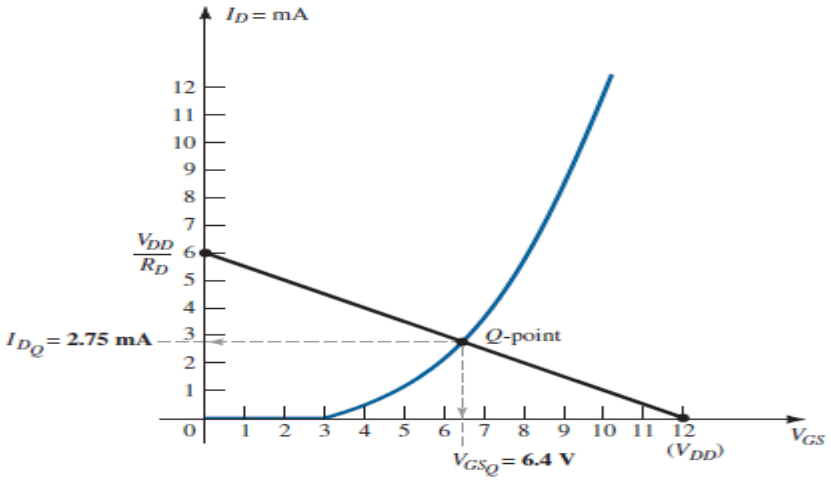


FIG. 42
Determining the Q-point for the network of Fig. 40.

8.2 Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 43. The fact that *IG* = 0 mA results in the following equation for *VGG* as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad (39)$$

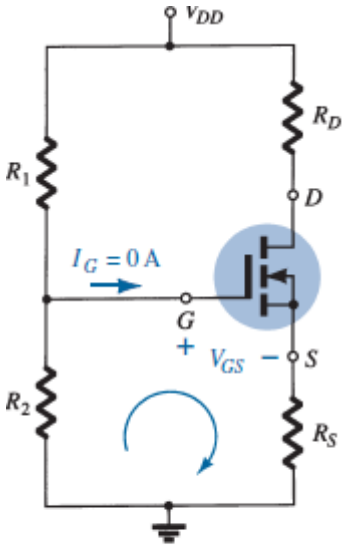


FIG. 43
Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.

Applying Kirchhoff's voltage law around the indicated loop of Fig. 43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$
$$V_{GS} = V_G - V_{R_S}$$
$$V_{GS} = V_G - I_D R_S$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$
$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$
$$V_{DS} = V_{DD} - I_D(R_S + R_D) \qquad (41)$$

Since the characteristics are a plot of *ID* versus *VGS* and Eq. (40) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once *IDQ* and *VGSQ* are known, all the remaining quantities of the network such as *VDS*, *VD*, and *VS* can be determined.

EXAMPLE 11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 44.

Solution:

Network

$$\text{Eq. (39):} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$$

$$\text{Eq. (40):} \quad V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

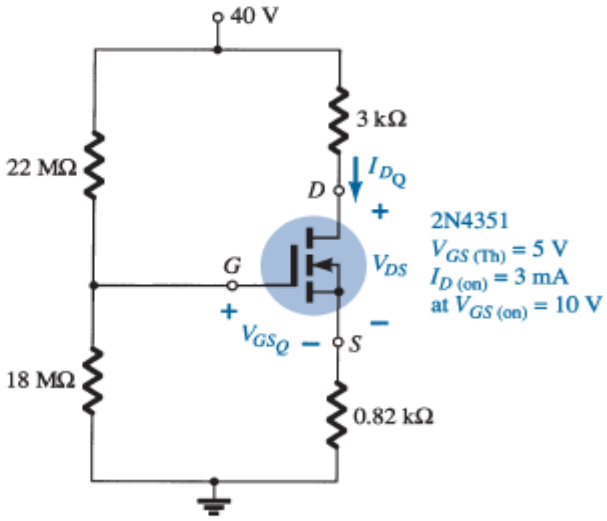


FIG. 44
Example 11.

When $I_D = 0$ mA,

$$V_{GS} = 18\,\text{V} - (0\,\text{mA})(0.82\,\text{k}\Omega) = 18\,\text{V}$$

as appearing on Fig. 45. When $V_{GS} = 0$ V,

$$V_{GS} = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

$$0 = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

$$I_D = \frac{18\,\text{V}}{0.82\,\text{k}\Omega} = 21.95\,\text{mA}$$

as appearing on Fig. 45.

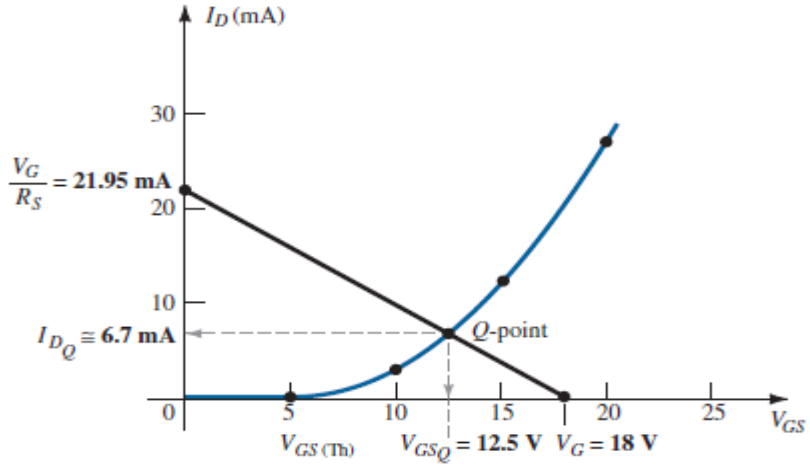


FIG. 45
Determining the Q-point for the network of Example 11.

Device

$$V_{GS(Th)} = 5\text{ V}, \quad I_{D(on)} = 3\text{ mA with } V_{GS(on)} = 10\text{ V}$$

$$\text{Eq. (34):} \quad k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

$$= \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

and

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

which is plotted on the same graph (Fig. 45). From Fig. 45,

$$I_{D_Q} \cong \mathbf{6.7\text{ mA}}$$

$$V_{GS_Q} = \mathbf{12.5\text{ V}}$$

$$\text{Eq. (41):} \quad V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\text{ V} - (6.7\text{ mA})(0.82\text{ k}\Omega + 3.0\text{ k}\Omega)$$

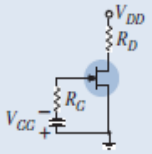
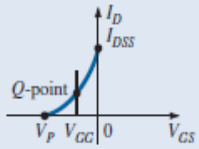
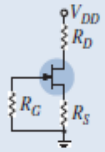
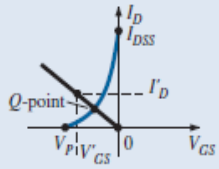
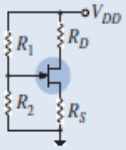
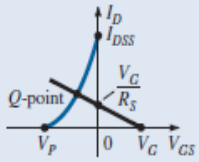
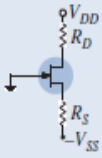
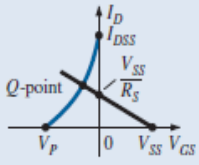
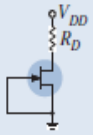
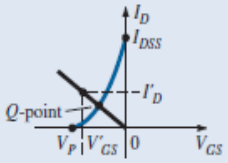
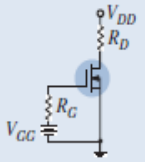
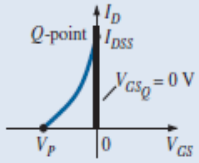
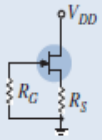
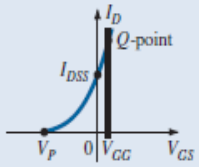
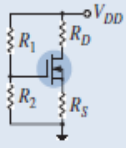
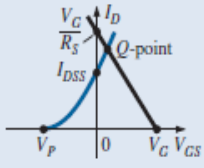
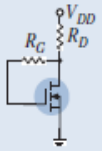
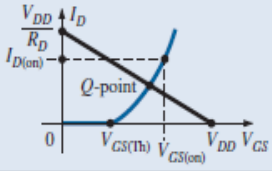
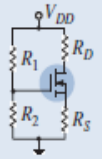
$$= 40\text{ V} - 25.6\text{ V}$$

$$= \mathbf{14.4\text{ V}}$$

9 Summary Table

Now that the dc analysis of a variety of BJT and FET configurations is established, the opportunity to analyze networks with both types of devices presents itself. Fundamentally, the analysis simply requires that we first approach the device that will provide a terminal voltage or current level. The door is then usually open to calculating other quantities and concentrating on the remaining unknowns. These are usually particularly interesting problems due to the challenge of finding the opening and then using the results of the past few sections to find the important quantities for each device. The equations and relationships used are simply those we have employed on more than one occasion—there is no need to develop any new methods of analysis.

TABLE 1
FET Bias Configurations

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
JFET Special case ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$