Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic II

Chapter 6

Lec6

Field-Effect Transistors

Prepared by

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7 Depletion-Type MOSFET

As noted in the introduction, there are three types of FETs: JFETs, MOSFETs, and MESFETs. MOSFETs are further broken down into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation; the name MOSFET stands for *m*etal–*o*xide–semiconductor *f*ield-*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections.

In this section we examine the depletion-type MOSFET, which has characteristics similar to those of a JFET between cutoff and saturation at *IDSS*, and also has the added feature of characteristics that extend into the region of opposite polarity for *VGS*.

7.1 Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 24. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation on which the device is constructed. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a type of insulator referred to as a *dielectric*. The fact that the SiO2 layer is an insulating layer means that:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

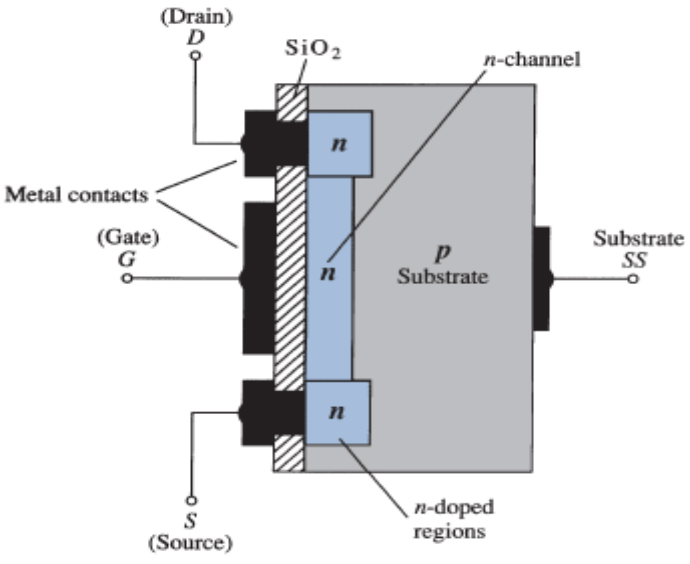

FIG. 24
n-Channel depletion-type MOSFET.

In addition:

It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is usually more than that of a typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. Because of the very high input impedance, the gate current *IG* is essentially 0 A for dcbiased configurations. The reason for the label metal–oxide–semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections; *oxide* for the silicon dioxide insulating layer; and *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and the channel has resulted in another name for the device: *insulated-gate FET*, or *IGFET*, although this label is used less and less in the literature.

7.2 Basic Operation and Characteristics

In Fig. 25 the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage *VDD* is applied across the drain-to-source terminals. The result is an attraction of the free electrons of the *n*-channel for the positive voltage at the drain. The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with *VGS* = 0V continues to be labeled *IDSS*, as shown in Fig. 26.

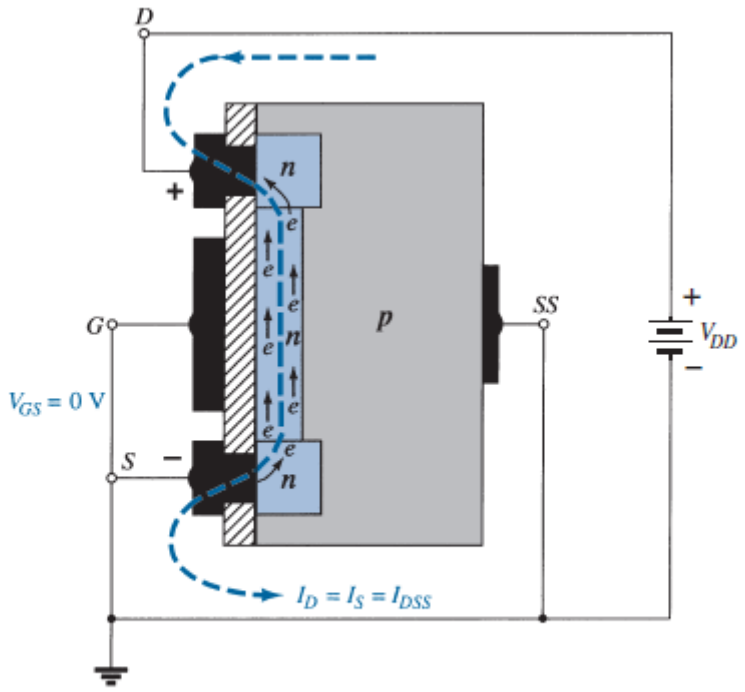

FIG. 25

n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.

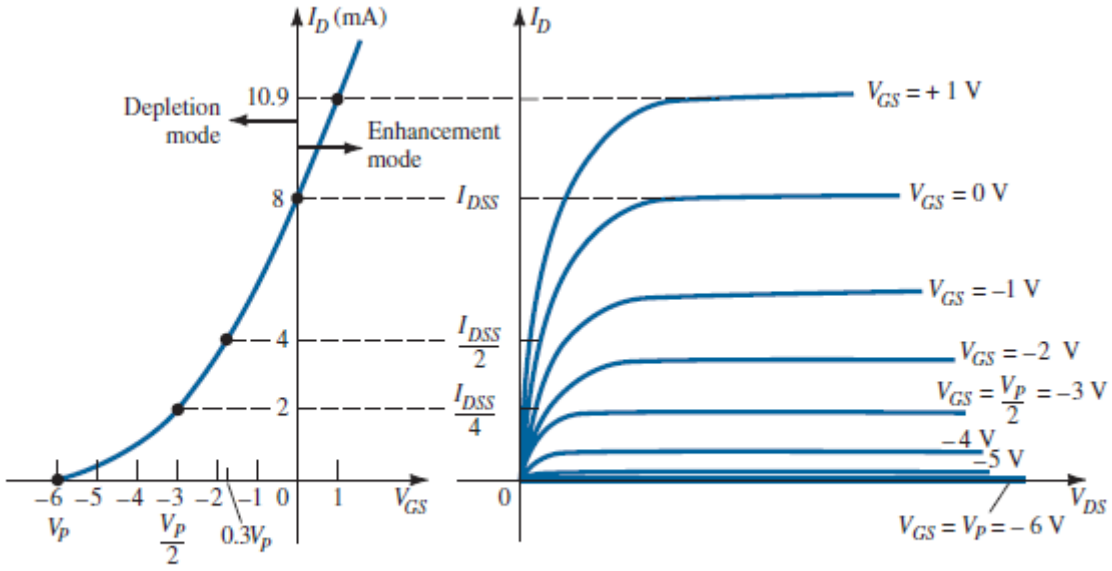

FIG. 26
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

In Fig. 27, VGS is set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 27. Depending on the magnitude of the negative bias established by *VGS*, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher is the rate of recombination.

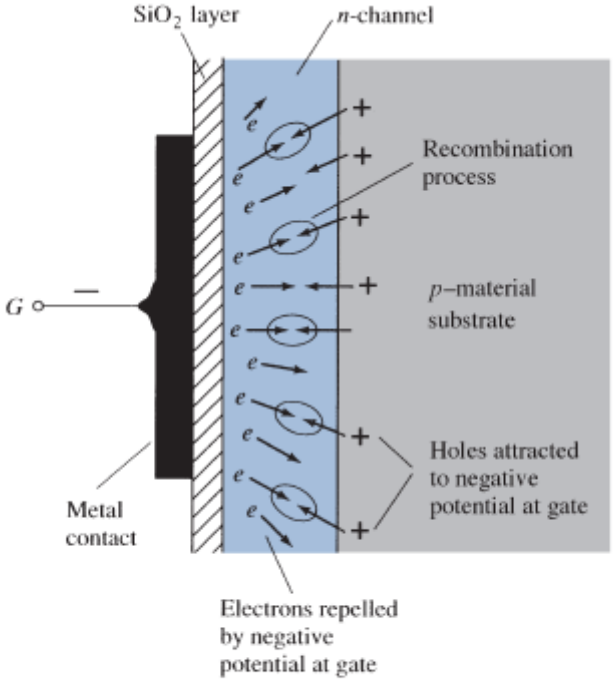

FIG. 27
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

The resulting level of drain current is therefore reduced with increasing negative bias for *VGS*, as shown in Fig. 26 for *VGS* = -1 V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.

For positive values of *VGS*, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 26 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the *VGS*= 0 V and *VGS* = +1 V curves of Fig. 26 is a clear indication of how much the current has increased for the 1-V change in *VGS*. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 26, the application of a voltage *VGS* = +4 V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with *VGS* =0V. For this reason, the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of *IDSS* referred to as the *depletion region.* It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with *VGS* in the equation and the sign be carefully monitored in the mathematical operations.

EXAMPLE 3 Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10\text{ mA}$ and $V_P = -4\text{ V}$.

Solution:

At $V_{GS} = 0\text{ V}$, $I_D = I_{DSS} = 10\text{ mA}$

$V_{GS} = V_P = -4\text{ V}$, $I_D = 0\text{ mA}$

$$V_{GS} = \frac{V_P}{2} = \frac{-4\text{ V}}{2} = -2\text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10\text{ mA}}{4} = 2.5\text{ mA}$$

and at $I_D = \frac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$$

all of which appear in Fig. 28.

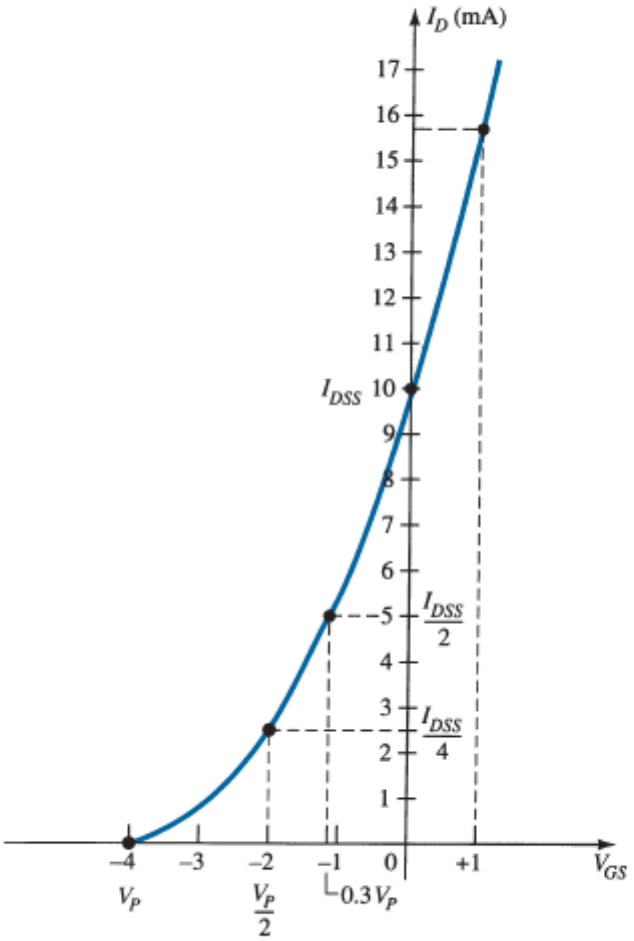

FIG. 28

Transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (10\text{ mA})\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = (10\text{ mA})\,(1 + 0.25)^2 = (10\text{ mA})\,(1.5625)$$

$$\cong 15.63\text{ mA}$$

which is sufficiently high to finish the plot.

7.3 P-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 24. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 29a. The terminals remain as identified, but all the voltage polarities and the current

directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 26, but with *VDS* having negative values, *ID* having positive values as indicated (since the defined direction is now reversed), and *VGS* having the opposite polarities as shown in Fig. 29c. The reversal in *VGS* will result in a mirror image (about the *ID* axis) for the transfer characteristics as shown in Fig. 29b. In other words, the drain current will increase from cutoff at *VGS = VP* in the positive *VGS* region to *IDSS* and then continue to increase for increasingly negative values of *VGS*. Shockley's equation is still applicable and requires simply placing the correct sign for both *VGS* and *VP* in the equation.

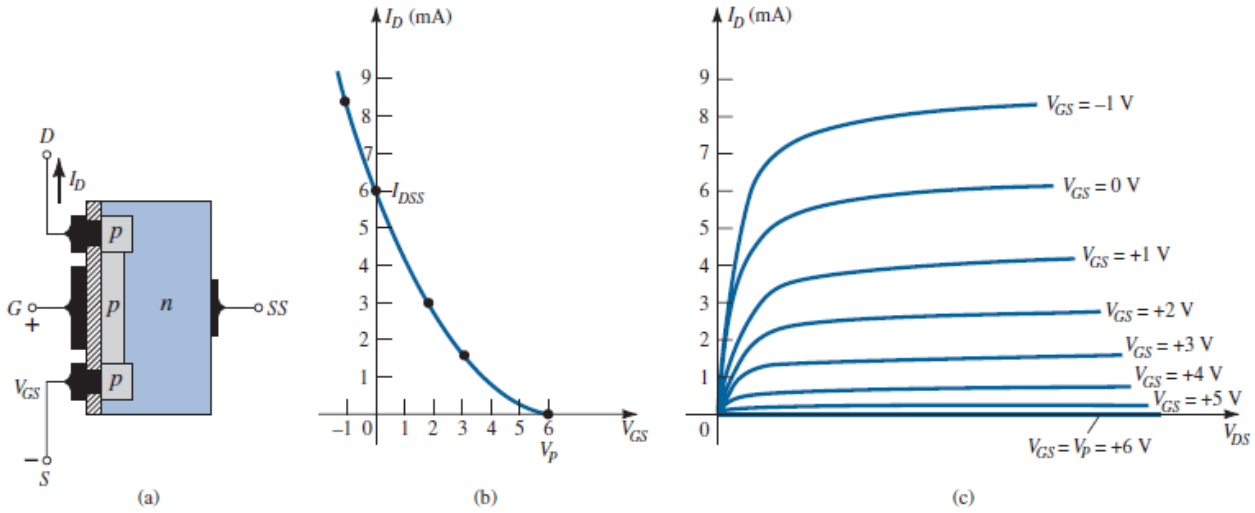

FIG. 29
p-Channel depletion-type MOSFET with I_{DSS} = 6 mA and V_P = +6 V.

7.4 Symbols, Specification Sheets, and Case Construction

The graphic symbols for an n- and p-channel depletion-type MOSFET are provided in Fig. 30. Note how the symbols chosen try to reflect the actual construction of the device. The lack of a direct connection (due to the gate insulation) between the gate and the channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and the source and is "supported" by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available, whereas in others it is not. For most of the analysis, the substrate and the source will be connected and the lower symbols will be employed.

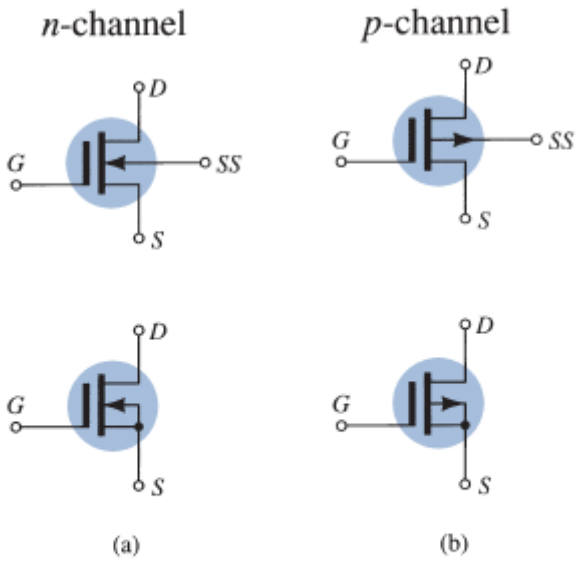

FIG. 30
Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.

8 Enhancement-Type MOSFET

Although there are some similarities in construction and mode of operation between depletion type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

8.1 Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 32. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, whereas in other cases a fourth lead (labeled SS) is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 32 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply

separated from a section of the *p*-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

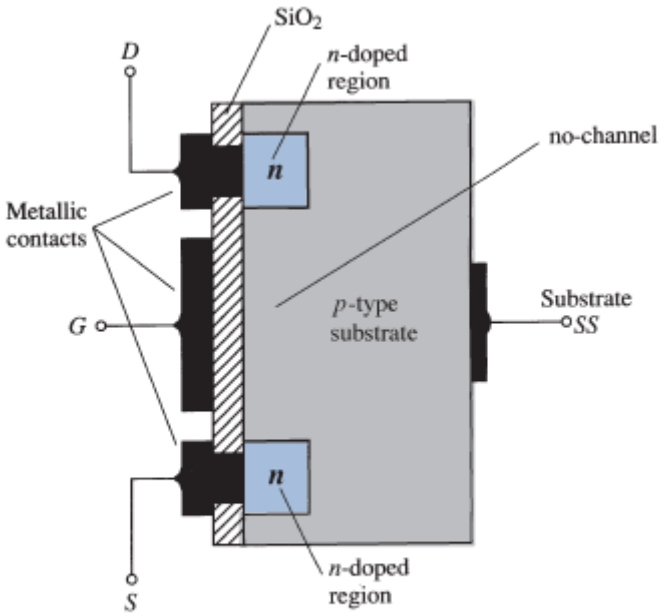

FIG. 32
n-Channel enhancement-type MOSFET.

8.2 Basic Operation and Characteristics

If *VGS* is set at 0 V and a voltage applied between the drain and the source of the device of Fig. 32, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively 0 A—quite different from the depletion-type MOSFET and JFET, where *ID* = *IDSS*. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the *n*-doped regions) if a path fails to exist between the two. With *VDS* some positive voltage, *VGS* at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p*–*n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source. In Fig. 33, both *VDS* and *VGS* have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO2 insulating layer void of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO2 layer.

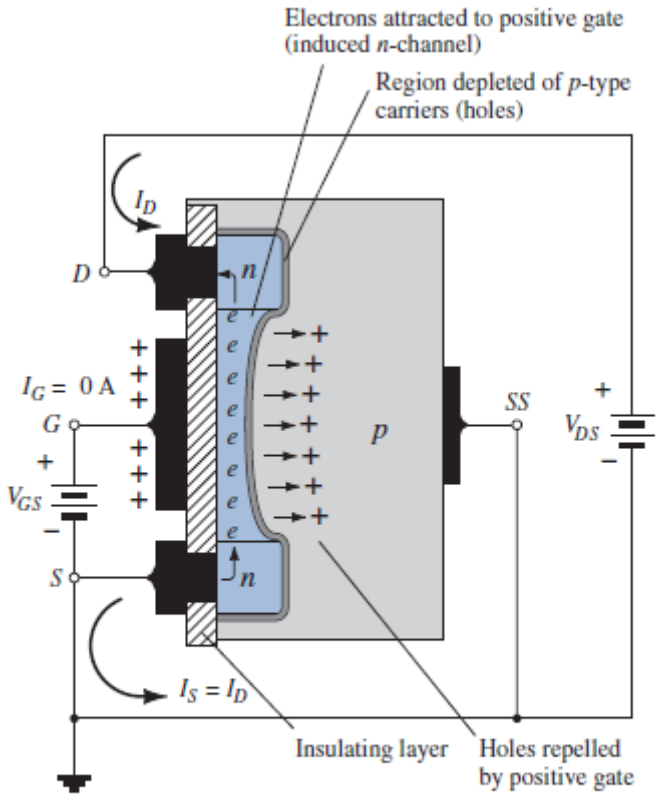

FIG. 33
Channel formation in the n-channel enhancement-type MOSFET.

The SiO2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As VGS increases in magnitude, the concentration of electrons near the SiO2 surface increases until eventually the induced n-type region can support a measurable flow between drain and source. The level of VGS that results in the significant increase in drain current is called the threshold voltage and is given the symbol VT. On specification sheets it is referred to as VGS(Th), although VT is less unwieldy and will be used in the analysis to follow. Since the channel is non-existent with VGS = 0 V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET. Both depletion- and enhancement type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

As VGS is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold VGS constant and increase the level of VDS, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of ID is due to a pinching-off process depicted by the narrower channel at the drain end of the

induced channel as shown in Fig. 34. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 34, we find that

$$V_{DG} = V_{DS} - V_{GS} \qquad (13)$$

If VGS is held fixed at some value such as 8 V and VDS is increased from 2 V to 5 V, the voltage VDG [by Eq. (13)] will increase from -6 V to -3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described

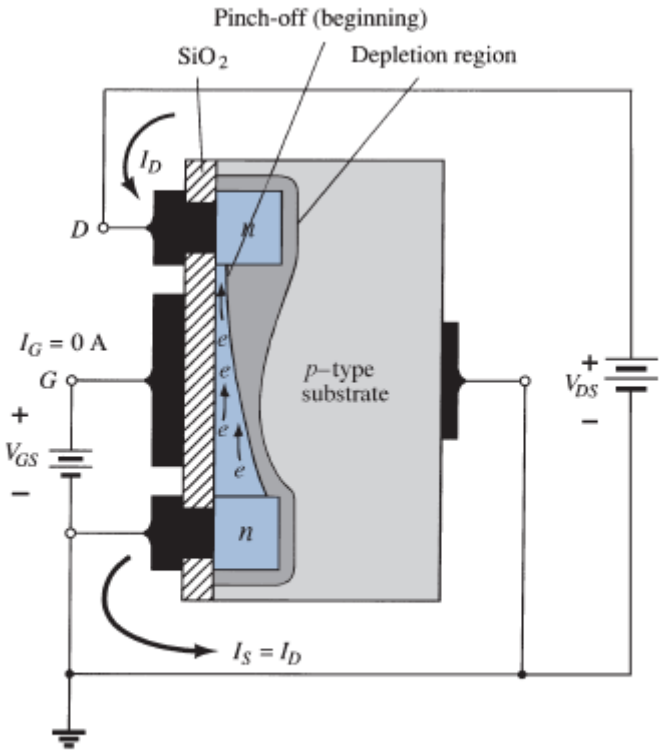

FIG. 34
Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}.

earlier for the JFET and depletion-type MOSFET. In other words, any further increase in *VDS* at the fixed value of *VGS* will not affect the saturation level of *ID* until breakdown conditions are encountered.

The drain characteristics of Fig. 35 reveal that for the device of Fig. 34 with *VGS* = 8 V, saturation occurs at a level of *VDS* = 6 V. In fact, the saturation level for *VDS* is related to the level of applied *VGS* by

$$V_{DS_{sat}} = V_{GS} - V_T \qquad (14)$$

Obviously, therefore, for a fixed value of *VT*, the higher the level of *VGS*, the greater is the saturation level for *VDS*, as shown in Fig. 34 by the locus of saturation levels.

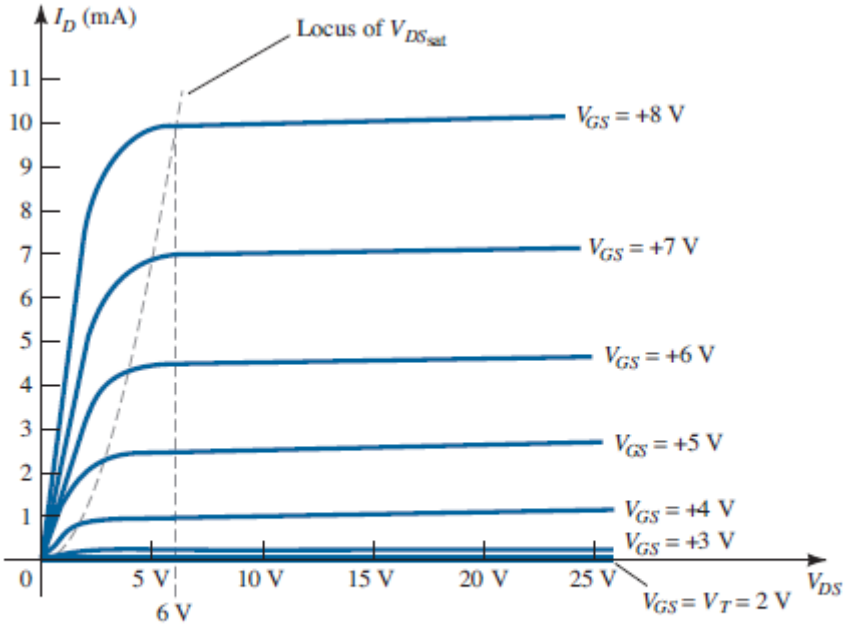

FIG. 35
Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V².

For values of VGS less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.

Figure 35 clearly reveals that as the level of *VGS* increases from *VT* to 8 V, the resulting saturation level for *ID* also increases from a level of 0 mA to 10 mA.

For levels of *VGS* 7 *VT*, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2 \qquad \textbf{(15)}$$

The value of *k* can be determined from the following equation [derived from Eq. (15)], where *ID*(on) and *VGS* (on) are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \qquad \textbf{(16)}$$

Substituting *ID*(on) = 10 mA when *VGS* (on) = 8 V from the characteristics of Fig. 35 Yields

$$k = \frac{10\text{ mA}}{(8\text{ V} - 2\text{ V})^2} = \frac{10\text{ mA}}{(6\text{ V})^2} = \frac{10\text{ mA}}{36\text{ V}^2}$$
$$= \mathbf{0.278 \times 10^{-3}\ A/V^2}$$

and a general equation for *ID* for the characteristics of Fig. 35 results in

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2\text{ V})^2$$

Substituting $V_{GS} = 4$ V, we find that

$$I_D = 0.278 \times 10^{-3}(4\text{ V} - 2\text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$
$$= 0.278 \times 10^{-3}(4) = \mathbf{1.11\ mA}$$

as verified by Fig. 35. At VGS = VT, the squared term is 0, and ID = 0 mA.

In Fig. 36, the drain and transfer characteristics have been set side by side to describe the transfer process from one to the other. Essentially, it proceeds as introduced earlier for the JFET and depletion-type MOSFETs. In this case, however, it must be remembered that the drain current is 0 mA for $VGS \leq VT$. As *VGS* is increased beyond *VT*, the drain current *ID* will begin to flow at an increasing rate in accordance with Eq. (15).

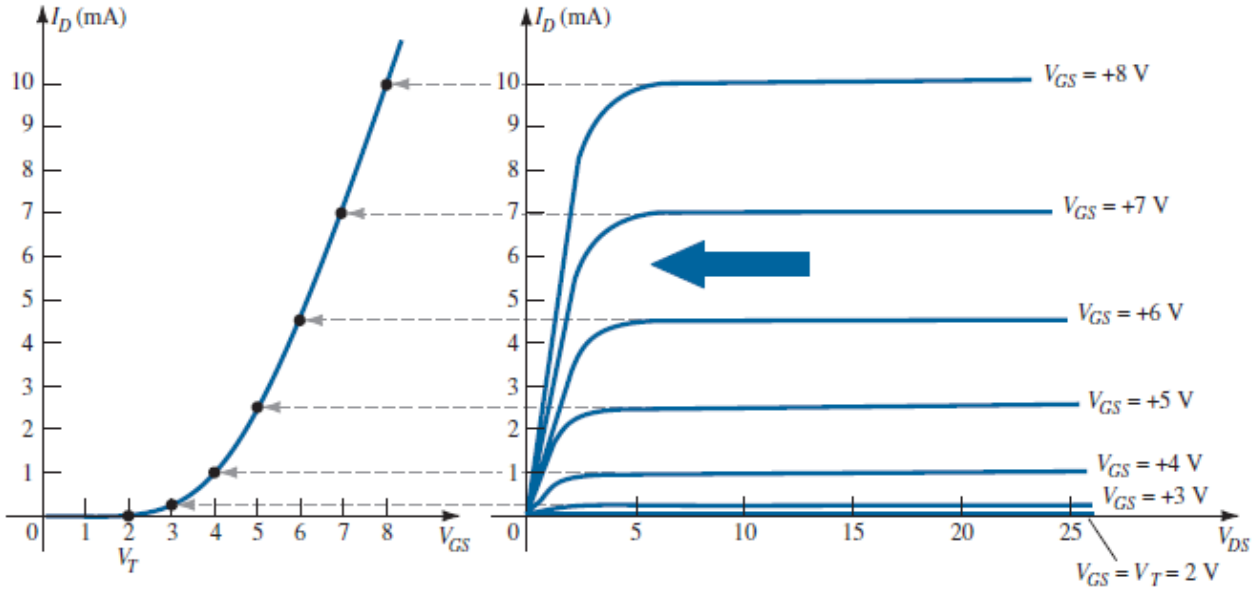

FIG. 36

Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

The transfer curve of Fig. 36 is certainly quite different from those obtained earlier. For an *n*-channel (induced) device, it is now totally in the positive *VGS* region and does not rise until *VGS* = *VT*. The question now surfaces as to how to plot the transfer characteristics given the levels of *k* and *VT* as included below for a particular MOSFET:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$$

First, a horizontal line is drawn at *ID* = 0 mA from *VGS* 5 0 V to *VGS* = 4 V as shown in Fig. 37a. Next, a level of *VGS* greater than *VT* such as 5 V is chosen and substituted into Eq. (15) to determine the resulting level of *ID* as follows: $I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$

$$= 0.5 \times 10^{-3}(5\text{ V} - 4\text{ V})^2 = 0.5 \times 10^{-3}(1)^2$$
$$= \mathbf{0.5\ mA}$$

and a point on the plot is obtained as shown in Fig. 37b. Finally, additional levels of *VGS* are chosen and the resulting levels of *ID* obtained. In particular, at *VGS* = 6, 7, and 8 V, the level of *ID* is 2, 4.5, and 8 mA, respectively, as shown on the resulting plot of Fig. 37c.

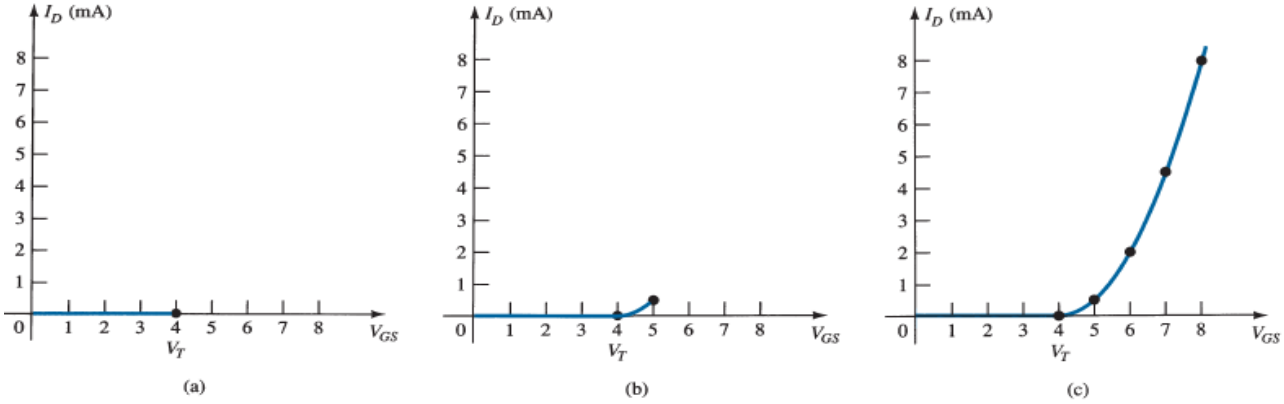

FIG. 37

Plotting the transfer characteristics of an n-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3}$ A/V² and $V_T = 4$ V.

8.3 P-Channel Enhancement-Type MOSFETS

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 32, as shown in Fig. 38a. That is, there is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 38c, with increasing levels of current resulting from increasingly negative values of *VGS*.

The transfer characteristics of Fig. 38b will be the mirror image (about the *ID* axis) of the transfer curve of Fig. 36, with *ID* increasing with increasingly negative values of *VGS* beyond *VT*, as shown in Fig. 38c. Equations (13) through (16) are equally applicable to *p*-channel devices

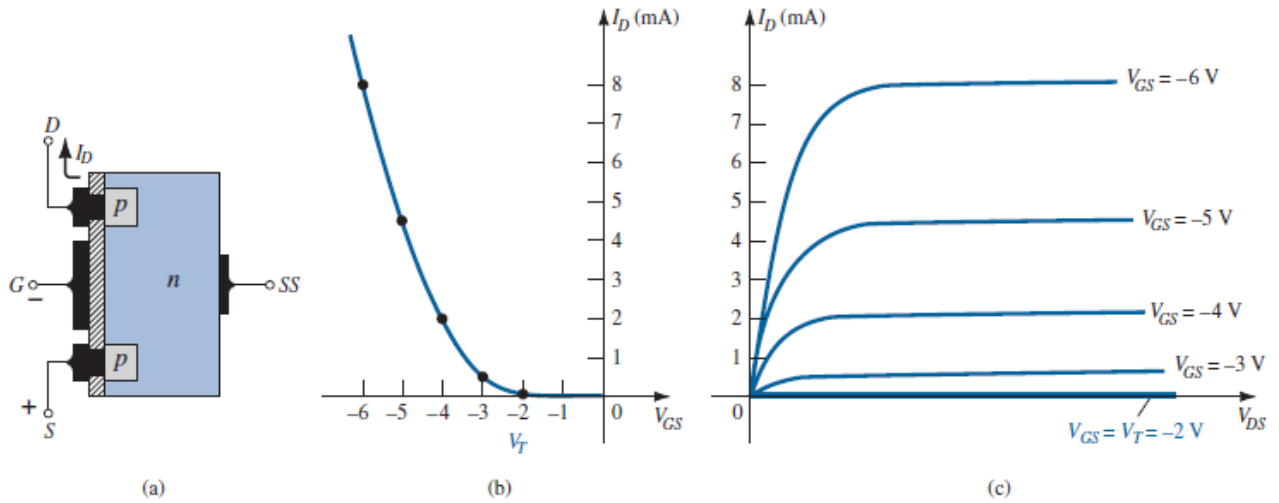

FIG. 38

p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V².

8.4 Symbols, Specification Sheets, and Case Construction

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 39. Again, note how the symbols try to reflect the actual construction of the device. The dashed line between drain and source is chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

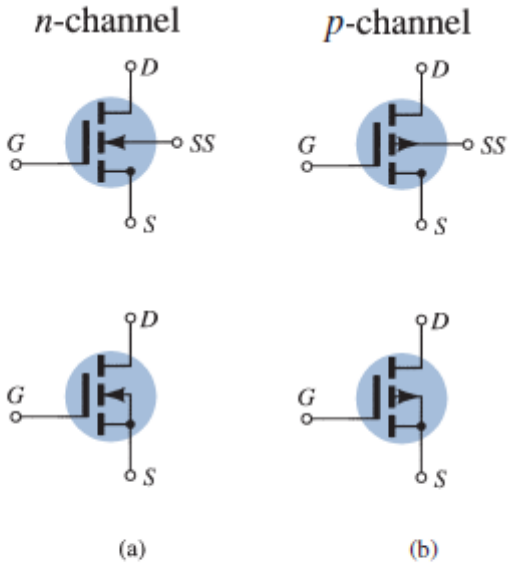

FIG. 39
Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.

The specification sheet for a Motorola *n*-channel enhancement-type MOSFET is provided as Fig. 40. The case construction and the terminal identification are provided next to the maximum ratings, which now include a maximum drain current of 30 mA dc. The specification sheet provides the level of *IDSS* under "off" conditions, which is now simply 10 nA dc (at *VDS* = 10 V and *VGS* = 0 V), compared to the milliampere range for the JFET and the depletion-type MOSFET. The threshold voltage is specified as *VGS*(Th) and has a range of 1 to 5 V dc, depending on the device employed. Rather than provide a range of *k* in Eq. (15), a typical level of *ID*(on) (3 mA in this case) is specified at a particular level of *VGS* (on) (10 V for the specified *ID* level). In other words, when *VGS* = 10 V, *ID* = 3 mA. The given levels of *VGS*(Th), *ID*(on), and *VGS* (on) permit a determination of *k* from Eq. (16) and a writing of the general equation for the transfer characteristics.

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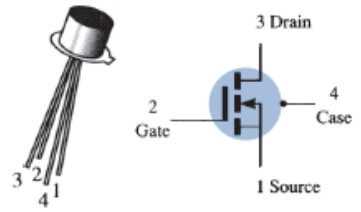
MOSFET SWITCHING



N-CHANNEL – ENHANCEMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10\ \mu A$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) $T_A = 25°C$ $T_A = 150°C$	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10\mu A$)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance ($V_{DS} = 10$ V, $I_D = 2.0$ mA, f = 1.0 kHz)	$\lvert y_{fs} \rvert$	1000	–	μmho
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)} = 10$ V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance ($V_{GS} = 10$ V, $I_D = 0$, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

($I_D = 2.0$ mAdc, $V_{DS} = 10$ Vdc, ($V_{GS} = 10$ Vdc) (See Figure 9; Times Circuit Determined))

FIG. 40

2N4351 Motorola n-channel enhancement-type MOSFET.

EXAMPLE 4 Using the data provided on the specification sheet of Fig. 40 and an average threshold voltage of $V_{GS(Th)} = 3$ V, determine:

a. The resulting value of k for the MOSFET.
b. The transfer characteristics.

Solution:

a. Eq. (16): $$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\text{ mA}}{(10\text{ V} - 3\text{ V})^2} = \frac{3\text{ mA}}{(7\text{ V})^2} = \frac{3 \times 10^{-3}}{49}\text{A/V}^2$$

$$= \mathbf{0.061 \times 10^{-3}\,A/V^2}$$

b. Eq. (15): $$I_D = k(V_{GS} - V_T)^2$$

$$= 0.061 \times 10^{-3}(V_{GS} - 3\text{ V})^2$$

For $V_{GS} = 5$ V,

$$I_D = 0.061 \times 10^{-3}(5\text{ V} - 3\text{ V})^2 = 0.061 \times 10^{-3}(2)^2$$

$$= 0.061 \times 10^{-3}(4) = 0.244\text{ mA}$$

For $V_{GS} = 8$, 10, 12, and 14 V, I_D will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 41.

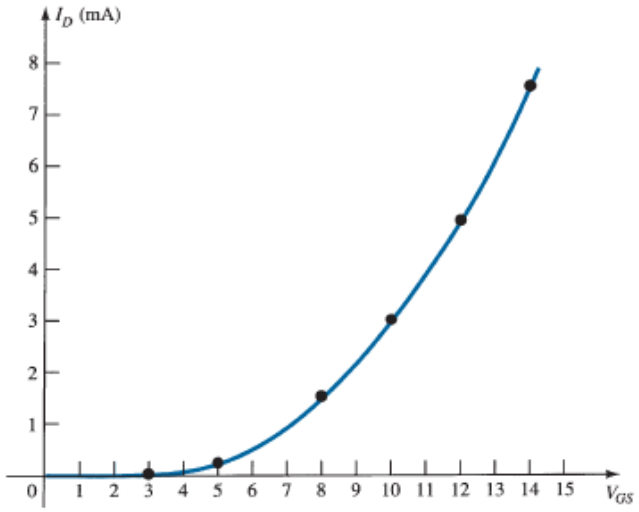


FIG. 41
Solution to Example 4.