Tikrit university

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Department of Electrical Engineering

Second Class

Electronic II

Chapter 6

Lec5

Field-Effect Transistors

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1 Introduction

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that:

The BJT transistor is a current-controlled device as depicted in Fig. 1a, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 1b.

In other words, the current IC in Fig. 1a is a direct function of the level of IB. For the FET the current ID will be a function of the voltage VGS applied to the input circuit as shown in Fig 1b. In each case the current of the output circuit is controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

Just as there are npn and pnp bipolar transistors, there are n-channel and p-channel field effect transistors. However, it is important to keep in mind that the BJT transistor is a bipolar device—the prefix bi indicates that the conduction level is a function of two charge carriers, electrons and holes. **The FET is a unipolar device depending solely on either electron (n-channel) or hole (p-channel) conduction.** The term field effect in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual ‘-contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet along the shortest path provided by the magnetic flux lines.

For the FET an electric field is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

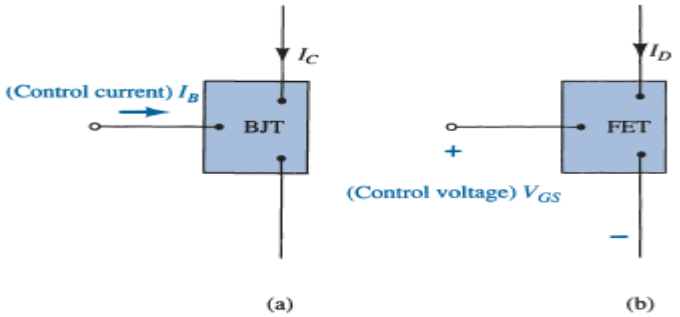

FIG. 1
(a) Current-controlled and (b) voltage-controlled amplifiers.

- ***One of the most important characteristics of the FET is its high input impedance.***

- ***Typical ac voltage gains for BJT amplifiers are a great deal more than for FETs.***
- ***FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.***

The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs. Three types of FETs are introduced in this chapter:

- the junction field-effect transistor (JFET),
- the metal–oxide–semiconductor field-effect transistor (MOSFET),
- the metal–semiconductor field-effect transistor (MESFET).

The MOSFET category is further broken down into depletion and enhancement types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design. However, as a discrete element in a typical top-hat container, it must be handled with care (to be discussed in a later section). The MESFET is a more recent development and takes full advantage of the high-speed characteristics of GaAs as the base semiconductor material. Although currently the more expensive option, the cost issue is often outweighed by the need for higher speeds in RF and computer designs.

2 Construction and Characteristics of JFETS

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two.

The basic construction of the *n*-channel JFET is shown in Fig. 3. Note that the major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D)*, whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).*

The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and the source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET

has two *p*–*n* junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. 3, that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is void of free carriers and is therefore unable to support conduction.

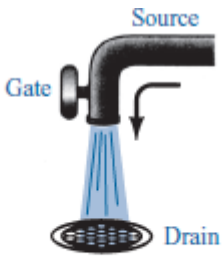

FIG. 4
Water analogy for the JFET control mechanism.

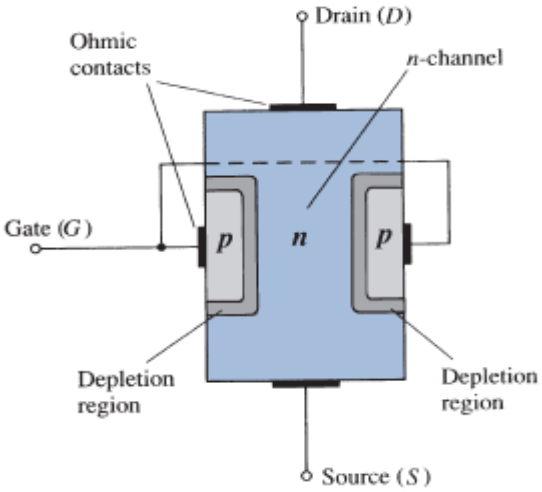

FIG. 3
Junction field-effect transistor (JFET).

The water analogy of Fig. 4 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source, which establishes a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain." The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 3 because the terminology is defined for electron flow.

2-1 VGS =0V, *VDS* some positive value

In Fig. 5, a positive voltage *VDS* is applied across the channel and the gate is connected directly to the source to establish the condition *VGS* 5 0 V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 3. The instant the voltage *VDD* (=*VDS*) is applied, the electrons are drawn to the drain terminal, establishing the conventional current *ID* with the defined direction of Fig. 5. The path of charge flow clearly reveals that the drain and source currents are equivalent (*ID* = *IS*). Under the conditions in Fig. 5, the flow of charge is relatively uninhibited and is limited solely by the resistance of

the *n*-channel between drain and source. It is important to note that the depletion region is wider near the top of both *p*-type materials. The reason for the change in width of the region is best described through the help of Fig. 6. Assuming a uniform resistance in the *n*-channel, we can break down the resistance of the channel into the divisions appearing in Fig. 6.

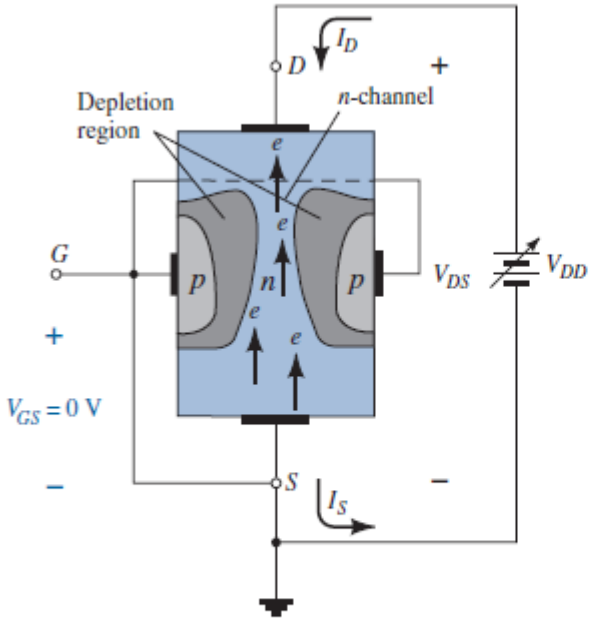

FIG. 5
JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

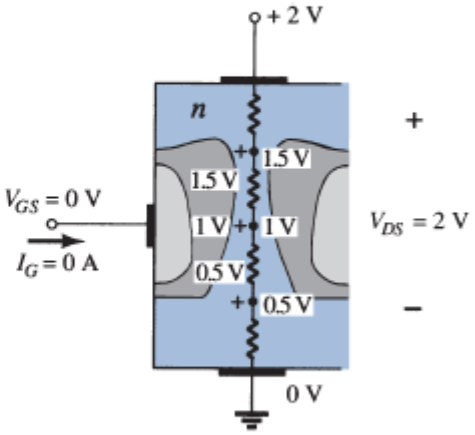

FIG. 6
Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

The current *ID* will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the *p*-type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V. Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider is the depletion region—hence the distribution of the depletion region as shown in Fig. 6. The fact that the *p–n* junction is reverse-biased for the length of the channel results in a gate current of zero amperes, as shown in the same figure. The fact that *IG* = 0 A is an important characteristic of the JFET.

As the voltage VDS is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of ID versus VDS will appear as shown in Fig. 7. The relative straightness of the plot reveals that for the region of low values of VDS, the resistance is essentially constant. As VDS increases and approaches a level referred to as VP in Fig. 7, the depletion regions of Fig. 5 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the

curve in the graph of Fig. 7 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If VDS is increased to a level where it appears that the two depletion regions would

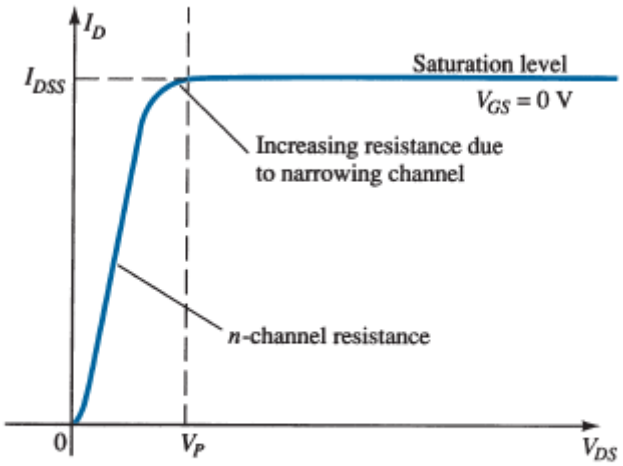

FIG. 7
I_D versus V_{DS} for $V_{GS} = 0$ V.

"touch" as shown in Fig. 8, a condition referred to as *pinch-off* will result. The level of *VDS* that establishes this condition is referred to as the *pinch-off voltage* and is denoted by *VP*, as shown in Fig. 7. In actuality, the term *pinch-off* is a misnomer in that it suggests the current *ID* is pinched off and drops to 0 A. As shown in Fig. 7, however, this is hardly the case— *ID* maintains a saturation level defined as *IDSS* in Fig. 7. In reality a very small channel still exists, with a current of very high density. The fact that *ID* does not drop off at pinch-off and maintains the saturation level indicated in Fig. 7 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p*–*n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

As *VDS* is increased beyond *VP*, the region of close encounter between the two depletion regions increase in length along the channel, but the level of *ID* remains essentially the same. In essence, therefore, once *VDS* 7 *VP* the JFET has the characteristics of a current source. As shown in Fig. 9, the current is fixed at *ID* = *IDSS*, but the voltage *VDS* (for levels 7 *VP*) is determined by the applied load. The choice of notation *IDSS* is derived from the fact that it is the *d*rain-to-*s*ource current with a *s*hort-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

IDSS is the maximum drain current for a JFET and is defined by the conditions VGS= 0 V and VDS > | VP | .

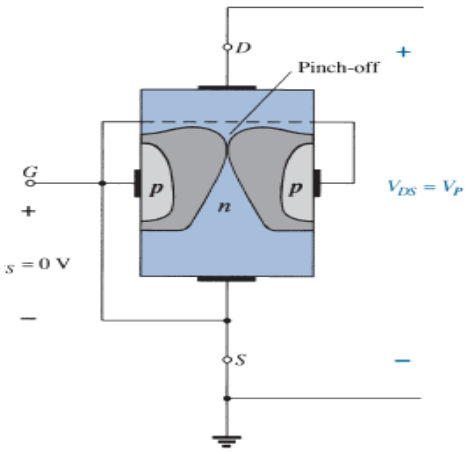

FIG. 8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

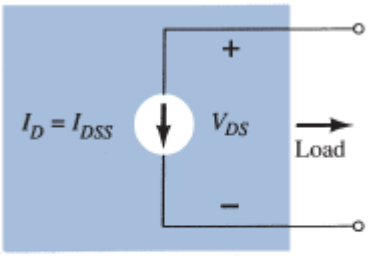

FIG. 9
Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

2.2 VGS < 0 v

The voltage from gate to source, denoted VGS, is the controlling voltage of the JFET. Just as various curves for IC versus VCE were established for different levels of IB for the BJT transistor, curves of ID versus VDS for various levels of VGS can be developed for the JFET. For the n-channel device the controlling voltage VGS is made more and more negative from its VGS 5 0 V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

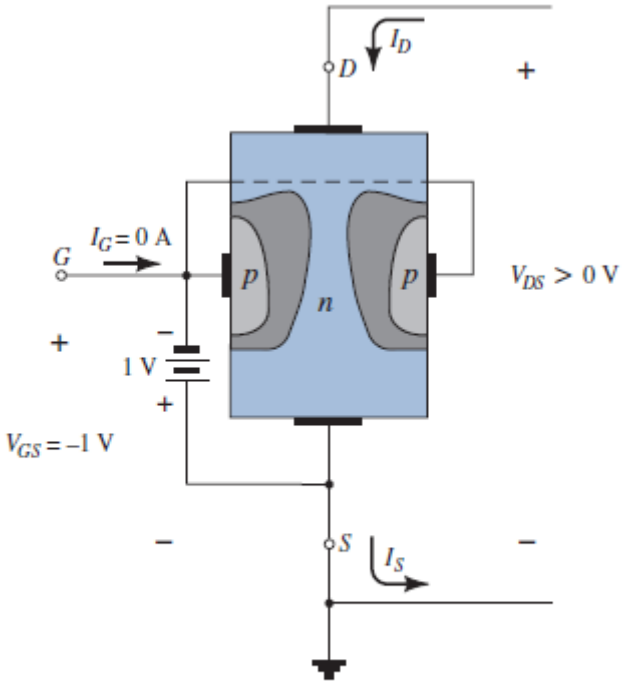

FIG. 10
Application of a negative voltage to the gate of a JFET.

In Fig. 10 a negative voltage of 21 V is applied between the gate and source terminals for a low level of *VDS*. The effect of the applied negative-bias *VGS* is to establish depletion regions similar to those obtained with *VGS* 5 0 V, but at lower levels of *VDS*. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of *VDS*, as shown in Fig. 11 for *VGS* = -1 V. The resulting saturation level for *ID* has been reduced and in fact will continue to decrease as *VGS* is made more and more negative. Note also in Fig. 11 how the pinch-off voltage continues to drop in a parabolic manner as *VGS* becomes more and more negative. Eventually, *VGS* when *VGS* = -*VP* will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

The level of VGS that results in ID = 0 mA is defined by VGS= VP, with VP being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

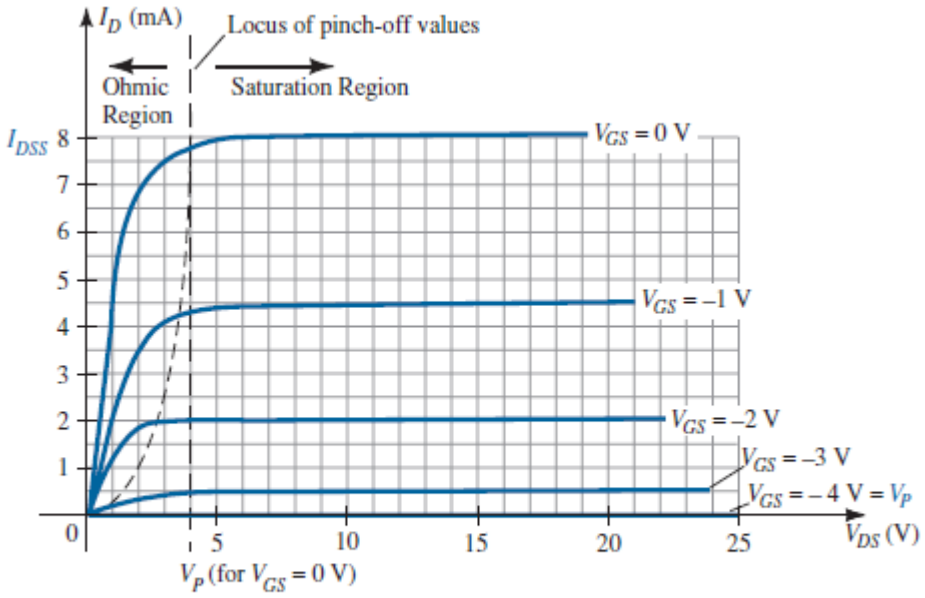

FIG. 11
n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

2-3 **voltage-Controlled resistor**

The region to the left of the pinch-off locus of Fig. 11 is referred to as the *ohmic* or *voltage-controlled resistance region*

The following equation provides a good first approximation to the resistance level in terms of the applied voltage *VGS*:

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \qquad (1)$$

where *ro* is the resistance with *VGS* 5 0 V and *rd* is the resistance at a particular level of *VGS*. For an *n*-channel JFET with *ro* = 10 kV (*VGS* = 0 V, *VP* = -6 V), Eq. (1) results in 40 kV at *VGS* = -3 V

2.4 p-Channel devices

The p-channel JFET is constructed in exactly the same manner as the n-channel device of Fig. 3 but with a reversal of the p- and n-type materials as shown in Fig. 12. The defined current directions are reversed, as are the actual polarities for the voltages VGS and VDS. For the p-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for VDS will result in negative voltages for VDS on the characteristics of Fig. 13, which has an IDSS of 6 mA and a pinch-off voltage of VGS = +6 V. Do not let the minus signs for VDS confuse you. They simply indicate that the source is at a higher potential than the drain.

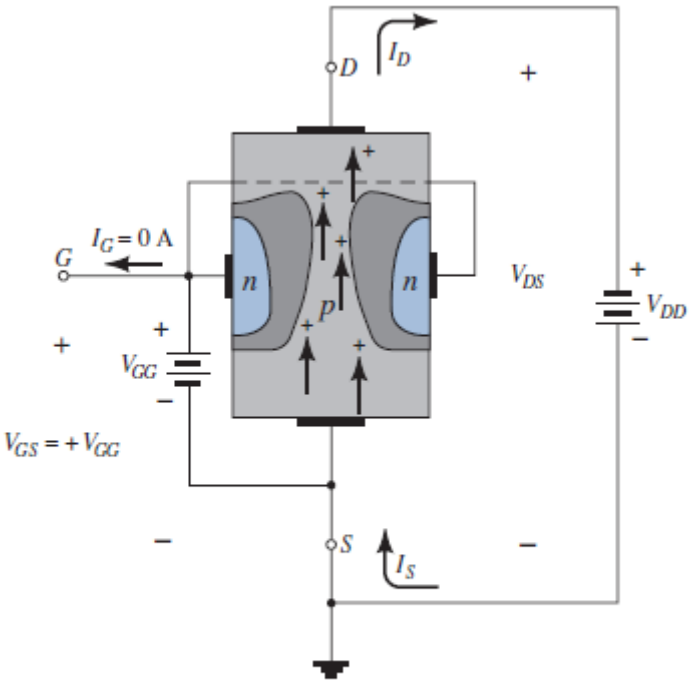

FIG. 12
p-Channel JFET.

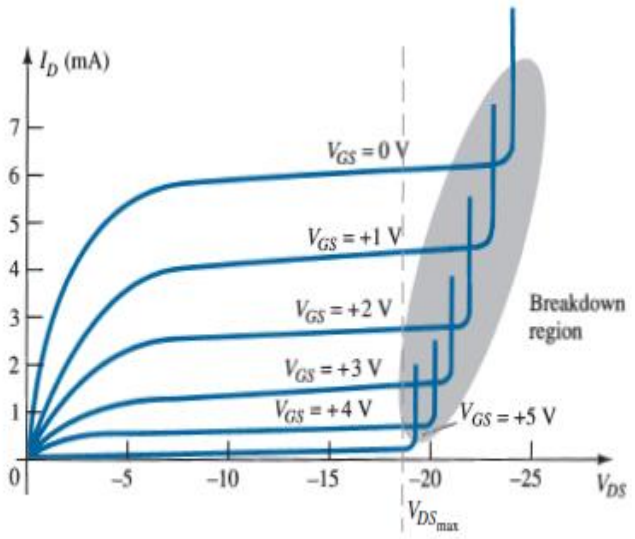

FIG. 13
p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

2.4 symbols

The graphic symbols for the n-channel and p-channel JFETs are provided in Fig. 14. Note that the arrow is pointing in for the n-channel device of Fig. 14a to represent the direction in which IG would flow if the p–n junction were forward-biased. For the p-channel device

(Fig. 14b) the only difference in the symbol is the direction of the arrow in the symbol.

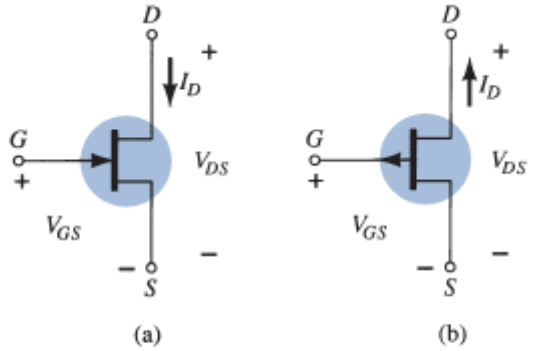

FIG. 14
JFET symbols: (a) n-channel; (b) p-channel.

2.5 summary

A number of important parameters and relationships were introduced in this section. A few that will surface frequently in the analysis to follow in this chapter and the next for *n*-channel

JFETs include the following:

- ***The maximum current is defined as IDSS and occurs when VGS = 0 V and VDS*** $\geq |VP|$***, as shown in Fig. 15a.***
- ***For gate-to-source voltages VGS is less than (more negative than) the pinch-off level, the drain current is 0 A (ID =0 A), as in Fig. 15b.***
- ***For all levels of VGS between 0 V and the pinch-off level, the current ID will range between IDSS and 0 A, respectively, as in Fig. 15c.***

A similar list can be developed for p-channel JFETs.

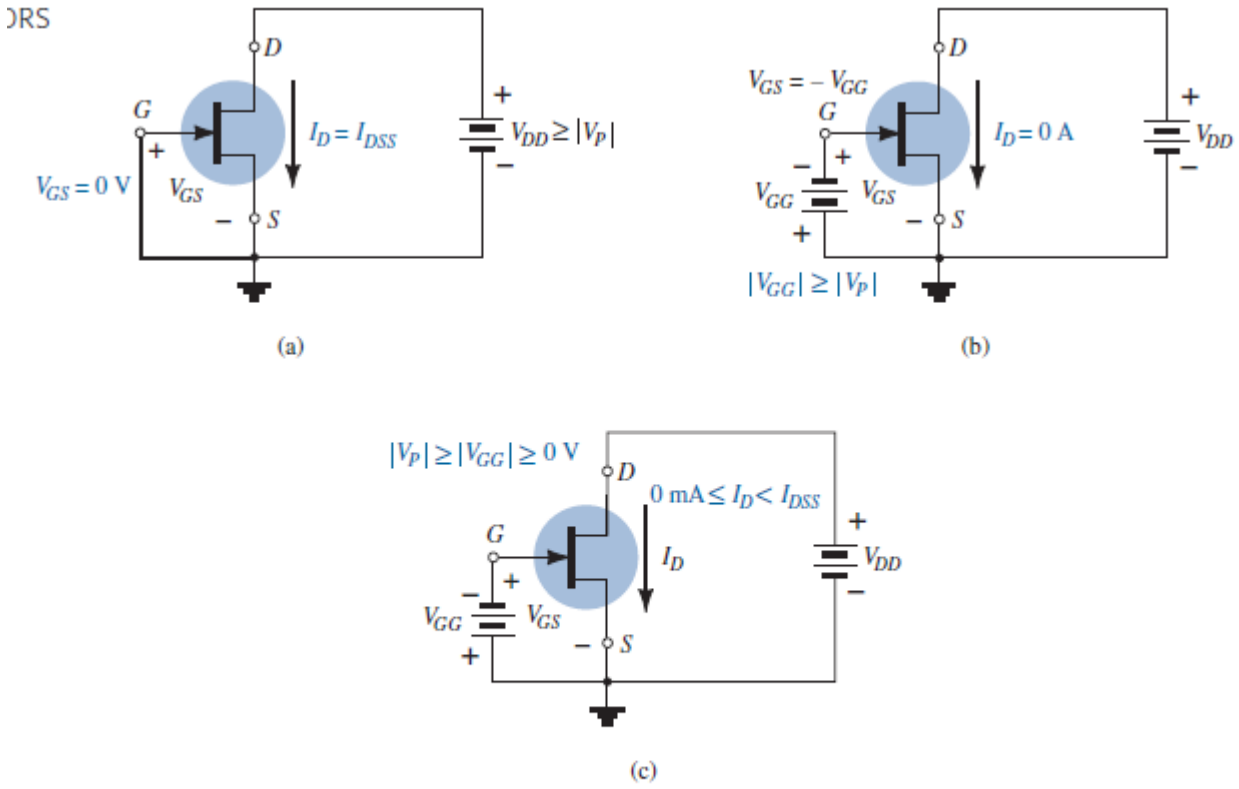

FIG. 15

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

3 Transfer Characteristics

3.1 Derivation

For the BJT transistor the output current IC and the input controlling current IB are related by beta, which was considered constant for the analysis to be performed. In equation form,

control variable

$$I_C = f(I_B) = \beta I_B \qquad (2)$$

constant

In Eq. (2) a linear relationship exists between IC and IB. Double the level of IB and IC will increase by a factor of two also. Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between ID and VGS is defined by Shockley's equation (see Fig. 16):

control variable

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (3)$$

constants

The squared term in the equation results in a nonlinear relationship between *ID* and *VGS*, producing a curve that grows exponentially with decreasing magnitude of *VGS*. For the dc analysis, a graphical rather than a mathematical approach will in general be more direct and easier to apply.

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 11. In Fig. 17 two graphs are provided, with the vertical scaling in milliamperes for each graph.

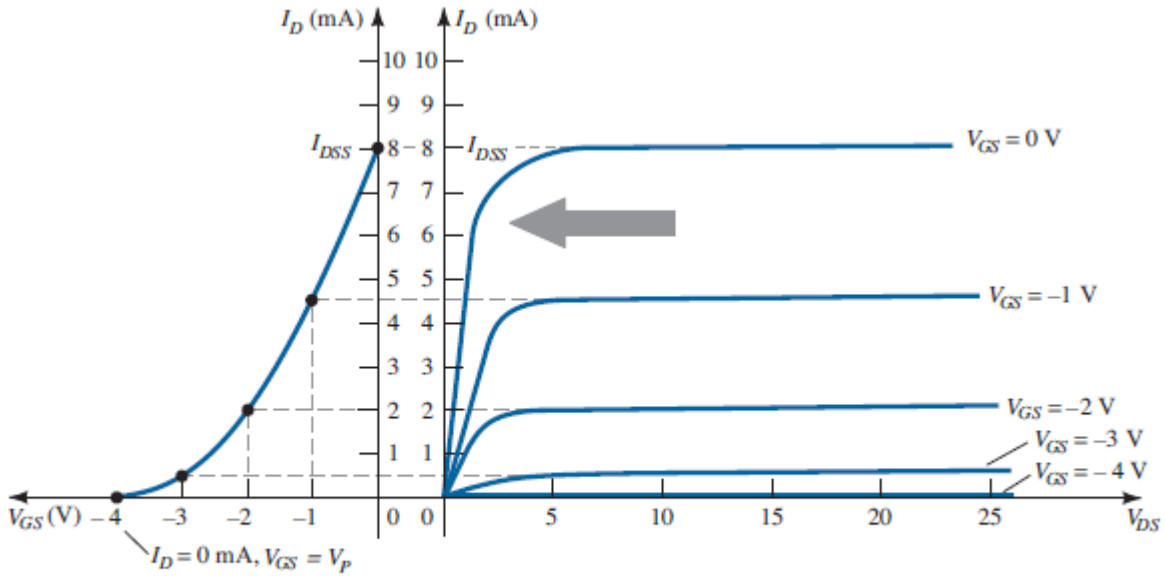

FIG. 17

Obtaining the transfer curve from the drain characteristics.

In review:

$$\boxed{\text{When } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS}} \tag{4}$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\boxed{\text{When } V_{GS} = V_P, \quad I_D = 0\text{ mA}} \tag{5}$$

3.2 Applying Shockley's Equation

The transfer curve of Fig. 17 can also be obtained directly from Shockley's equation (3) given simply the values of *IDSS* and *VP*. The levels of *IDSS* and *VP* define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points. The validity of Eq. (3) as a source of the transfer curve of Fig. 17 is best demonstrated by

examining a few specific levels of one variable and finding the resulting level of the other as follows:

Substituting *VGS*= 0 V gives

$$\text{Eq. (3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$\boxed{I_D = I_{DSS}\,|_{V_{GS}=0\,\text{V}}} \qquad (6)$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$
$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$\boxed{I_D = 0\,\text{A}\,|_{V_{GS}=V_P}} \qquad (7)$$

For the drain characteristics of Fig. 17, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 8\,\text{mA}\left(1 - \frac{-1\,\text{V}}{-4\,\text{V}}\right)^2 = 8\,\text{mA}\left(1 - \frac{1}{4}\right)^2 = 8\,\text{mA}\,(0.75)^2$$
$$= 8\,\text{mA}\,(0.5625)$$
$$= \mathbf{4.5\,mA}$$

Conversely, by using basic algebra we can obtain [from Eq. (3)] an equation for the resulting level of *VGS* for a given level of *ID*. The derivation is quite straightforward and results in

$$\boxed{V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)} \qquad (8)$$

Let us test Eq. (8) by finding the level of VGS that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 17. We find

$$V_{GS} = -4\,\text{V}\left(1 - \sqrt{\frac{4.5\,\text{mA}}{8\,\text{mA}}}\right)$$
$$= -4\,\text{V}(1 - \sqrt{0.5625}) = -4\,\text{V}(1 - 0.75)$$
$$= -4\,\text{V}(0.25)$$
$$= \mathbf{-1\,V}$$

3.3 Shorthand Method

Since the transfer curve must be plotted so frequently, it would be quite advantageous to have a shorthand method for plotting the curve in the quickest, most efficient manner while maintaining an acceptable degree of accuracy. The format of Eq. (3) is such that specific levels of *VGS* will result in levels of *ID* that can be memorized to provide the plot points needed to sketch the transfer curve. If we specify *VGS* to be one-half the pinch-off value *VP*, the resulting level of *ID* will be the following, as determined by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$
$$= I_{DSS}(0.25)$$

$$\boxed{I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS} = V_P/2}} \qquad (9)$$

Now it is important to realize that Eq. (9) is not for a particular level of *VP*. It is a general equation for any level of *VP* as long as *VGS* = *VP*>2. The result specifies that the drain current will always be one-fourth the saturation level *IDSS* as long as the gate-to-source voltage is one-half the pinch-off value. Note the level of *ID* for *VGS* = *VP*/2 = -4 V/2 = -2V in Fig. 17. If we choose *ID* = *IDSS*/2 and substitute into Eq. (8), we find that

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$
$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

$$\boxed{V_{GS} \cong 0.3V_P\big|_{I_D = I_{DSS}/2}} \qquad (10)$$

Additional points can be determined, but the transfer curve can be sketched to a satisfactory level of accuracy simply using the four plot points defined above and reviewed in Table 1..

TABLE 1
V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

EXAMPLE 1 Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

Solution: Two plot points are defined by

$$I_{DSS} = \mathbf{12\ mA} \quad \text{and} \quad V_{GS} = \mathbf{0\ V}$$

and

$$I_D = \mathbf{0\ mA} \quad \text{and} \quad V_{GS} = V_P$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\ V}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\ mA}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\ mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\ V}$. All four plot points are well defined on Fig. 18 with the complete transfer curve.

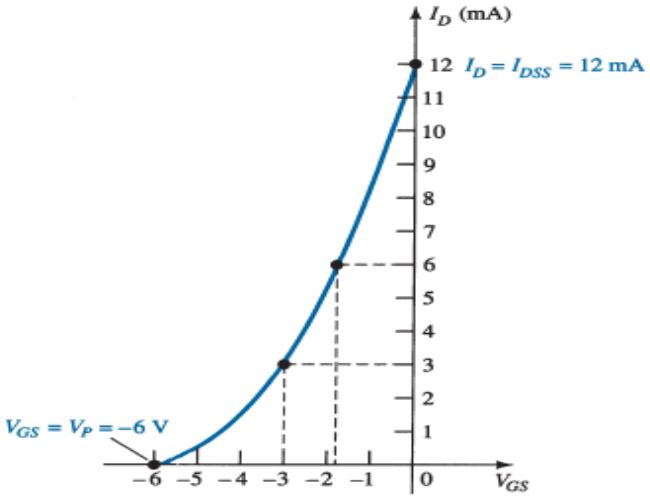

FIG. 18
Transfer curve for Example 1.

For *p*-channel devices Shockley's equation (3) can still be applied exactly as it appears. In this case, both *VP* and *VGS* will be positive and the curve will be the mirror image of the transfer curve obtained with an *n*-channel and the same limiting values.

EXAMPLE 2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\ V}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\ mA}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\ mA}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\ V}$. Both plot points appear in Fig. 19 along with the points defined by I_{DSS} and V_P.

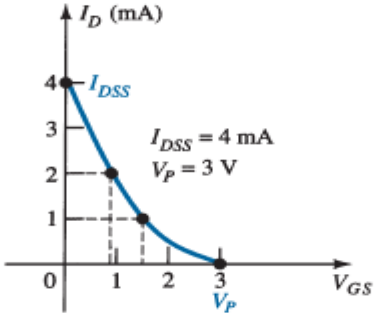

FIG. 19
Transfer curve for the p-channel device of Example 2.