Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic II

Chapter 5

Lec3

BJT AC Analysis

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15 Two-Port Systems Approach

In the design process, it is often necessary to work with the terminal characteristics of a device rather than the individual components of the system. In other words, the designer is handed a packaged product with a list of data regarding its characteristics but has no access to the internal construction. This section will relate the important parameters determined for a number of configurations in the previous sections to the important parameters of this packaged system. The result will be an understanding of how each parameter of the packaged system relates to the actual amplifier or network. The system of Fig. 61 is called a two-port system because there are two sets of terminals—one at the input and the other at the output. At this point it is particularly important to realize that ***the data surrounding a packaged system is the no-load data.*** This should be fairly obvious because the load has not been applied, nor does it come with the load attached to the package.

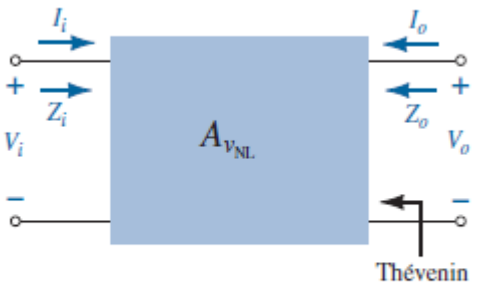

FIG. 61
Two-port system.

For the two-port system of Fig. 61 the polarity of the voltages and the direction of the currents are as defined. If the currents have a different direction or the voltages have a different polarity from that appearing in Fig. 61, a negative sign must be applied. Note again the use of the label AV_{NL} to indicate that the provided voltage gain will be the no load value.

For amplifiers the parameters of importance have been sketched within the boundaries of the two-port system as shown in Fig. 62. The input and output resistance of a packaged amplifier are normally provided along with the no-load gain. They can then be inserted as shown in Fig. 62 to represent the seated package.

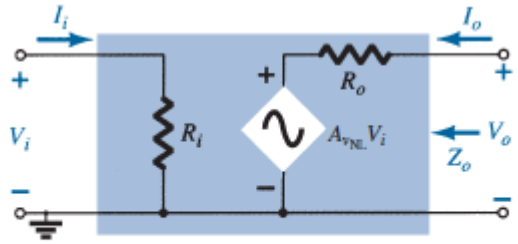

FIG. 62
Substituting the internal elements for the two-port system of Fig. 61.

For the no-load situation the output voltage is

$$V_o = A_{v_{NL}} V_i \qquad (86)$$

due to the fact that $I = 0A$, resulting in $IoRo = 0V$.

The output resistance is defined by $Vi = 0V$. Under such conditions the quantity (AV_{NL} Vi) is zero volts also and can be replaced by a short-circuit equivalent. The result is

$$Z_o = R_o \qquad (87)$$

Finally, the input impedance Zi simply relates the applied voltage to the resulting input current and

$$Z_i = R_i \qquad (88)$$

For the no-load situation, the current gain is undefined because the load current is zero. There is, however, a no-load voltage gain equal to AVNL. The effect of applying a load to a two-port system will result in the configuration of Fig. 63. Ideally, all the parameters of the model are unaffected by changing loads and levels of source resistance. However, for some transistor configurations the applied load can affect the input resistance, whereas for others the output resistance can be affected by the source resistance.

In all cases, however, by simple definition, the no-load gain is unaffected by the application of any load. In any case, once AV_{NL}, Ri, and Ro are defined for a particular configuration, the equations about to be derived can be employed.

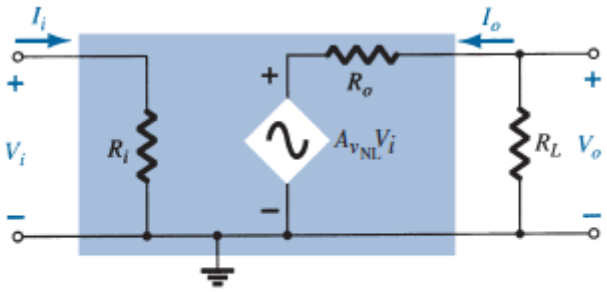

FIG. 63
Applying a load to the two-port system of Fig. 62.

Applying the voltage-divider rule to the output circuit results in

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

and

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}} \qquad (89)$$

Because the ratio *RL*/ (*RL* + *Ro*) is always less than 1, we have further evidence that the loaded voltage gain of an amplifier is always less than the no-load level. The current gain is then determined by

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i}\frac{Z_i}{R_L}$$

and

$$\boxed{A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}} \qquad (90)$$

as obtained earlier. In general, therefore, the current gain can be obtained from the voltage gain and impedance parameters *Zi* and *RL*. The next example will demonstrate the usefulness

and validity of Eqs. (89) and (90).

Our attention will now turn to the input side of the two-port system and the effect of an internal source resistance on the gain of an amplifier. In Fig. 64, a source with an internal resistance has been applied to the basic two-port system. The definitions of *Zi* and AV_{NL} are such that:

The parameters Zi and AV_{NL} of a two-port system are unaffected by the internal resistance of the applied source.

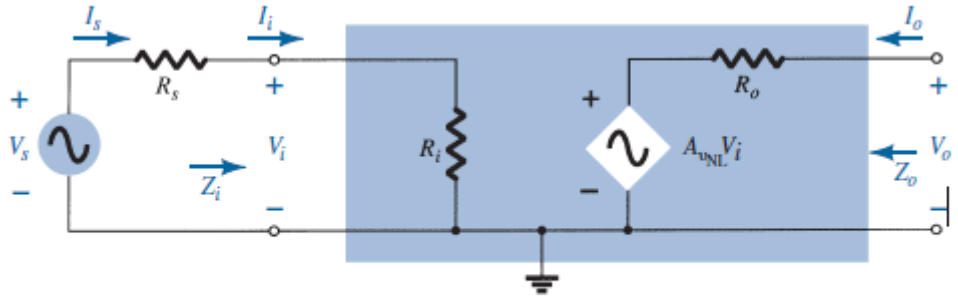

FIG. 64
Including the effects of the source resistance R_s.

However: *The output impedance may be affected by the magnitude of Rs.* The fraction of the applied signal reaching the input terminals of the amplifier of Fig. 64 is determined by the voltage-divider rule. That is,

$$V_i = \frac{R_i V_s}{R_i + R_s} \qquad (91)$$

Equation (91) clearly shows that the larger the magnitude of *Rs*, the lower is the voltage at the input terminals of the amplifier. In general, therefore, as mentioned earlier, for a particular amplifier, the larger the internal resistance of a signal source, the lower is the overall gain of the system. For the two-port system of Fig. 64,

$$V_o = A_{v_{NL}} V_i$$

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

so that

$$V_o = A_{v_{NL}} \frac{R_i}{R_i + R_s} V_s$$

and

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}} \qquad (92)$$

The effects of *Rs* and *RL* have now been demonstrated on an individual basis. The next natural question is how the presence of both factors in the same network will affect the total gain. In Fig. 65, a source with an internal resistance *Rs* and a load *RL* have been applied to a two-port system for which the parameters *Zi*, AV_{NL}, and *Zo* have been specified. For the moment, let us assume that *Zi* and *Zo* are unaffected by *RL* and *Rs*, respectively.

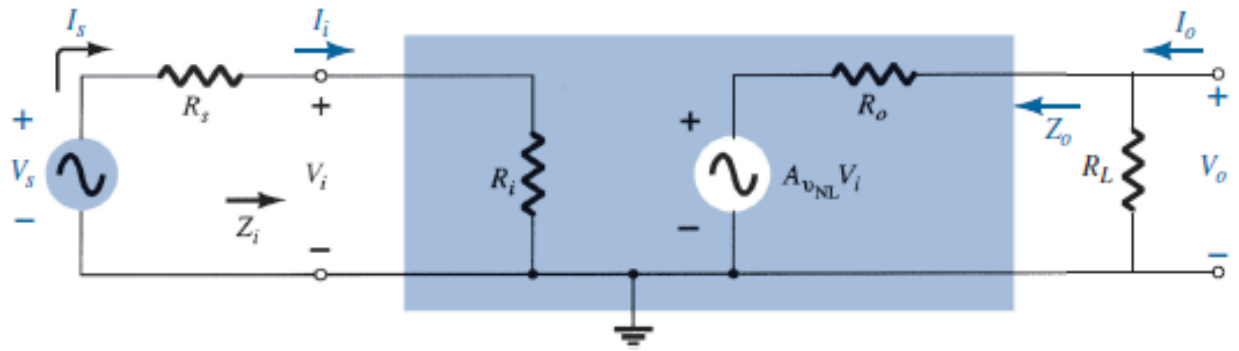

FIG. 65

Considering the effects of R_s and R_L on the gain of an amplifier.

At the input side we find

$$\text{Eq. (91):} \quad V_i = \frac{R_i V_s}{R_i + R_s}$$

or

$$\boxed{\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}} \tag{93}$$

and at the output side,

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{NL}} V_i$$

or

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{NL}} \tag{94}$$

For the total gain $A_{v_s} = V_o/V_s$, the following mathematical steps can be performed:

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}} \tag{95}$$

and substituting Eqs. (93) and (94) results in

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}} \tag{96}$$

Because $I_i = V_i/R_i$, as before,

$$\boxed{A_{i_L} = -A_{v_L} \frac{R_i}{R_L}} \tag{97}$$

or, using $I_s = V_s/(R_s + R_i)$,

$$\boxed{A_{i_s} = -A_{v_s} \frac{R_s + R_i}{R_L}} \tag{98}$$

However, *Ii* = *Is*, so Eqs. (97) and (98) generate the same result. Equation (96) clearly reveals that both the source and the load resistance will reduce the overall gain of the system.

The two reduction factors of Eq. (96) form a product that has to be carefully considered in any design procedure. It is not sufficient to ensure that *Rs* is relatively small if the effect of the magnitude of *RL* is ignored. For instance, in Eq. (96), if the first factor is 0.9 and the second factor is 0.2, the product of the two results in an overall reduction factor equal to (0.9) (0.2) = 0.18, which is close to the lower factor. The effect of the excellent 0.9 level was completely wiped out by the significantly lower second multiplier. If both were 0.9-level factors, the net result would be (0.9)(0.9)= 0.81, which is still quite high. Even if the first were 0.9 and the second 0.7, the net result of 0.63 would still be respectable. In general, therefore, for good overall gain the effects of *Rs* and *RL* must be evaluated individually and as a product.

EXAMPLE 12 Determine A_{v_L} and A_{v_s} for the network of Example 11 and compare solutions. Example 1 showed that $A_{v_{NL}} = -280$, $Z_i = 1.07\ \text{k}\Omega$, and $Z_o = 3\ \text{k}\Omega$. In Example 11, $R_L = 4.7\ \text{k}\Omega$ and $R_s = 0.3\ \text{k}\Omega$.

Solution:

a. Eq. (89): $$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{NL}}$$
$$= \frac{4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}(-280.11)$$
$$= \mathbf{-170.98}$$
as in Example 11.

b. Eq. (96): $$A_{v_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}$$
$$= \frac{1.07\ \text{k}\Omega}{1.07\ \text{k}\Omega + 0.3\ \text{k}\Omega} \cdot \frac{4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}(-280.11)$$
$$= (0.781)(0.610)(-280.11)$$
$$= \mathbf{-133.45}$$
as in Example 11.

EXAMPLE 13 Given the packaged (no-entry-possible) amplifier of Fig. 66:

a. Determine the gain A_{v_L} and compare it to the no-load value with $R_L = 1.2\ \text{k}\Omega$.
b. Repeat part (a) with $R_L = 5.6\ \text{k}\Omega$ and compare solutions.
c. Determine A_{v_s} with $R_L = 1.2\ \text{k}\Omega$.
d. Find the current gain $A_i = \dfrac{I_o}{I_i} = \dfrac{I_o}{I_s}$ with $R_L = 5.6\ \text{k}\Omega$.

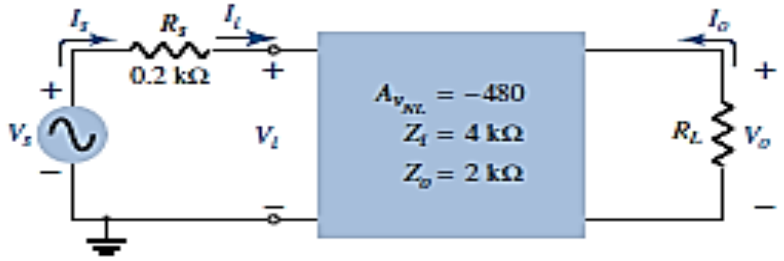

FIG. 66
Amplifier for Example 13.

Solution:

a. Eq. (89): $A_{v_L} = \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{1.2\ \text{k}\Omega}{1.2\ \text{k}\Omega + 2\ \text{k}\Omega}(-480) = (0.375)(-480)$$

$$= \mathbf{-180}$$

which is a dramatic drop from the no-load value.

b. Eq. (89): $A_{v_L} = \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{5.6\ \text{k}\Omega}{5.6\ \text{k}\Omega + 2\ \text{k}\Omega}(-480) = (0.737)(-480)$$

$$= \mathbf{-353.76}$$

which clearly reveals that the larger the load resistor, the better is the gain.

c. Eq. (96): $A_{v_s} = \dfrac{R_i}{R_i + R_s} \cdot \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{4\ \text{k}\Omega}{4\ \text{k}\Omega + 0.2\ \text{k}\Omega} \cdot \frac{1.2\ \text{k}\Omega}{1.2\ \text{k}\Omega + 2\ \text{k}\Omega}(-480)$$

$$= (0.952)(0.375)(-480)$$

$$= \mathbf{-171.36}$$

which is fairly close to the loaded gain A_v because the input impedance is considerably more than the source resistance. In other words, the source resistance is relatively small compared to the input impedance of the amplifier.

d. $A_{i_L} = \dfrac{I_o}{I_i} = \dfrac{I_o}{I_s} = -A_{v_L}\dfrac{Z_i}{R_L}$

$$= -(-353.76)\left(\frac{4\ \text{k}\Omega}{5.6\ \text{k}\Omega}\right) = (-353.76)(0.714)$$

$$= \mathbf{-252.6}$$

16 Cascaded Systems

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 67, where *AV*1, *AV*2, *AV*3, and so on, are the voltage gains of each stage *under loaded conditions.* That is, *AV*1 is determined with the *input impedance to AV*2 *acting as the load on AV*1. For *AV*2, *AV*1 will determine the signal strength and source impedance at the input to *AV*2. The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots \tag{99}$$

and the total current gain is given by

$$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} \tag{100}$$

No matter how perfect the system design, the application of a succeeding stage or load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where *AV*1, *AV*2, and so on, of Fig. 67 are simply the no-load values. The no-load parameters can be used to determine the loaded gains of each stage, but Eq. (99) requires the loaded values. The load on stage 1 is *Zi*2, on stage 2 *Zi*3, on stage 3 *Zin*, and so on.

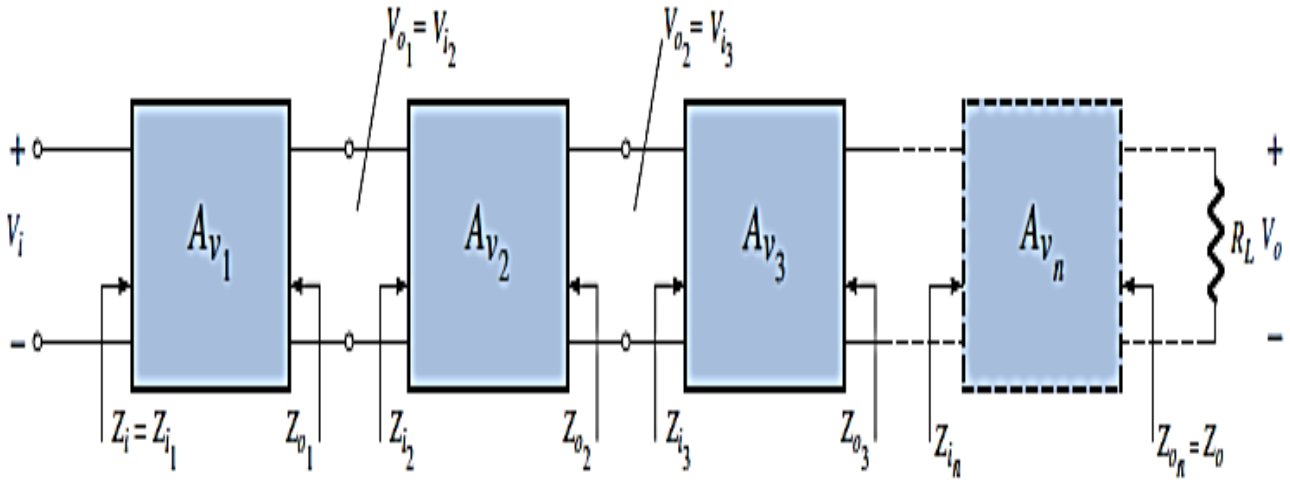

FIG. 67
Cascaded system.

EXAMPLE 14 The two-stage system of Fig. 68 employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of the applied signal appears at the input terminals of the common-base amplifier. In Fig. 68, the no-load values are provided for each system, with the exception of Z_i and Z_o for the emitter-follower, which are the loaded values. For the configuration of Fig. 68, determine:

a. The loaded gain for each stage.
b. The total gain for the system, A_v and A_{v_s}.
c. The total current gain for the system.
d. The total gain for the system if the emitter-follower configuration were removed.

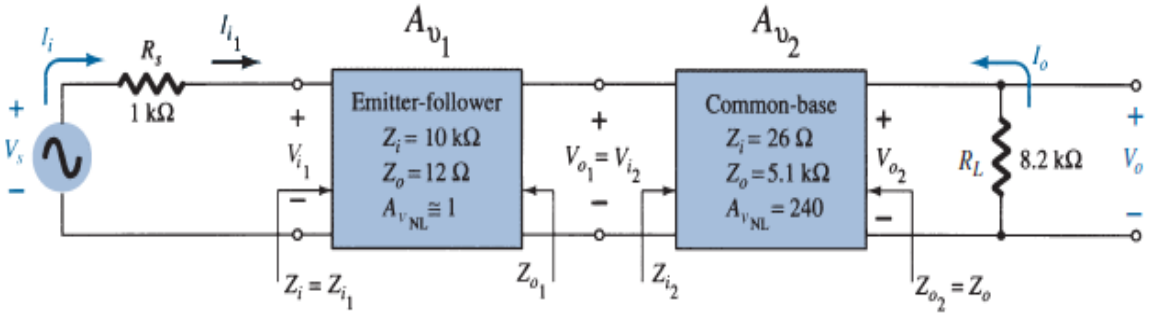

FIG. 68
Example 14.

Solution:

a. For the emitter-follower configuration, the loaded gain is (by Eq. (94))

$$V_{o_1} = \frac{Z_{i_2}}{Z_{i_2} + Z_{o_1}} A_{v_{NL}} V_{i_1} = \frac{26\ \Omega}{26\ \Omega + 12\ \Omega}(1)\, V_{i_1} = 0.684\, V_{i_1}$$

and $$A_{V_i} = \frac{V_{o_1}}{V_{i_1}} = \mathbf{0.684}$$

For the common-base configuration,

$$V_{o_2} = \frac{R_L}{R_L + R_{o_2}} A_{v_{NL}} V_{i_2} = \frac{8.2\,\text{k}\Omega}{8.2\,\text{k}\Omega + 5.1\,\text{k}\Omega}(240)\, V_{i_2} = 147.97\, V_{i_2}$$

and $$A_{v_2} = \frac{V_{o_2}}{V_{i_2}} = \mathbf{147.97}$$

b. Eq. (99): $A_{v_T} = A_{v_1} A_{v_2}$
$= (0.684)(147.97)$
$= \mathbf{101.20}$

Eq. (91): $$A_{v_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s} A_{v_T} = \frac{(10\,\text{k}\Omega)(101.20)}{10\,\text{k}\Omega + 1\,\text{k}\Omega}$$
$$= \mathbf{92}$$

c. Eq. (100): $$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} = -(101.20)\left(\frac{10\,\text{k}\Omega}{8.2\,\text{k}\Omega}\right)$$
$$= \mathbf{-123.41}$$

d. Eq. (91): $$V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s} V_s = \frac{26\ \Omega}{26\ \Omega + 1\,\text{k}\Omega} V_s = 0.025\ V_s$$

and $$\frac{V_i}{V_s} = 0.025 \quad \text{with} \quad \frac{V_o}{V_i} = 147.97 \quad \text{from above}$$

and $$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = (0.025)(147.97) = \mathbf{3.7}$$

16.1 RC-Coupled BJT amplifiers

One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. 69 in the next example. The name is derived from the capacitive coupling capacitor *Cc* and the fact that the load on the first stage is an *RC* combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

EXAMPLE 15

a. Calculate the no-load voltage gain and output voltage of the *RC*-coupled transistor amplifiers of Fig. 69.
b. Calculate the overall gain and output voltage if a 4.7 kΩ load is applied to the second stage, and compare to the results of part (a).
c. Calculate the input impedance of the first stage and the output impedance of the second stage.

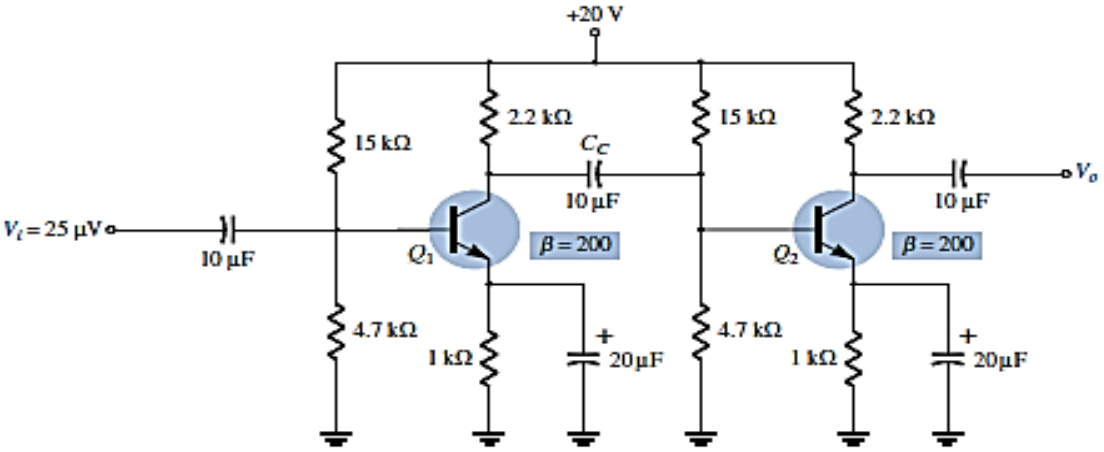

FIG. 69
RC-coupled BJT amplifier for Example 15.

Solution:

a. The dc bias analysis results in the following for each transistor:

$$V_B = 4.7\text{ V}, \quad V_E = 4.0\text{ V}, \quad V_C = 11\text{ V}, \quad I_E = 4.0\text{ mA}$$

At the bias point,

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4\text{ mA}} = 6.5\ \Omega$$

The loading of the second stage is

$$Z_{i_2} = R_1 \| R_2 \| \beta r_e$$

which results in the following gain for the first stage:

$$A_{v_1} = -\frac{R_C \| (R_1 \| R_2 \| \beta r_e)}{r_e}$$

$$= -\frac{(2.2\text{ k}\Omega) \| [15\text{ k}\Omega \| 4.7\text{ k}\Omega \| (200)(6.5\ \Omega)]}{6.5\ \Omega}$$

$$= -\frac{665.2\ \Omega}{6.5\ \Omega} = -102.3$$

For the unloaded second stage the gain is

$$A_{v_{2(\text{NL})}} = -\frac{R_C}{r_e} = -\frac{2.2\text{ k}\Omega}{6.5\ \Omega} = -338.46$$

resulting in an overall gain of

$$A_{v_{T(\text{NL})}} = A_{v_1} A_{v_{2(\text{NL})}} = (-102.3)(-338.46) \cong \mathbf{34.6 \times 10^3}$$

The output voltage is then

$$V_o = A_{v_{T(\text{NL})}} V_i = (34.6 \times 10^3)(25\ \mu\text{V}) \cong \mathbf{865\text{ mV}}$$

b. The overall gain with the 4.7-kΩ load applied is

$$A_{v_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_{T(\text{NL})}} = \frac{4.7\text{ k}\Omega}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega}(34.6 \times 10^3) \cong \mathbf{23.6 \times 10^3}$$

which is considerably less than the unloaded gain because R_L is relatively close to R_C.

$$V_o = A_{v_T} V_i$$

$$= (23.6 \times 10^3)(25\ \mu\text{V})$$

$$= \mathbf{590\text{ mV}}$$

c. The input impedance of the first stage is

$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 4.7\text{ k}\Omega \| 15\text{ k}\Omega \| (200)(6.5\ \Omega) = \mathbf{953.6\ \Omega}$$

whereas the output impedance for the second stage is

$$Z_{o_2} = R_C = \mathbf{2.2\text{ k}\Omega}$$

16.2 Cascode Connection

The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 70; the second is shown in Fig. 71 in the following example.

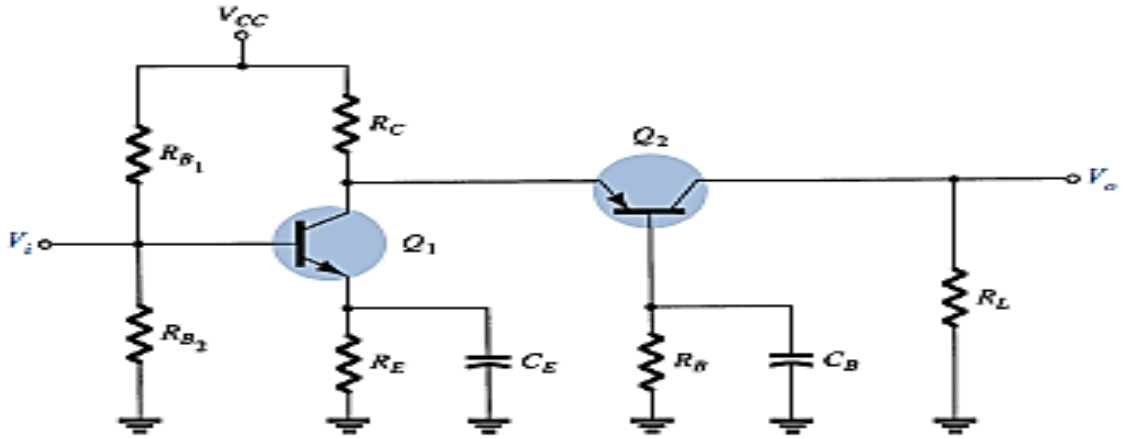

FIG. 70
Cascode configuration.

The arrangements provide a relatively high-input impedance with low voltage gain for the first stage to ensure the input Miller capacitance is at a minimum, whereas the following CB stage provides an excellent high-frequency response.

EXAMPLE 16 Calculate the no-load voltage gain for the cascode configuration of Fig. 71.

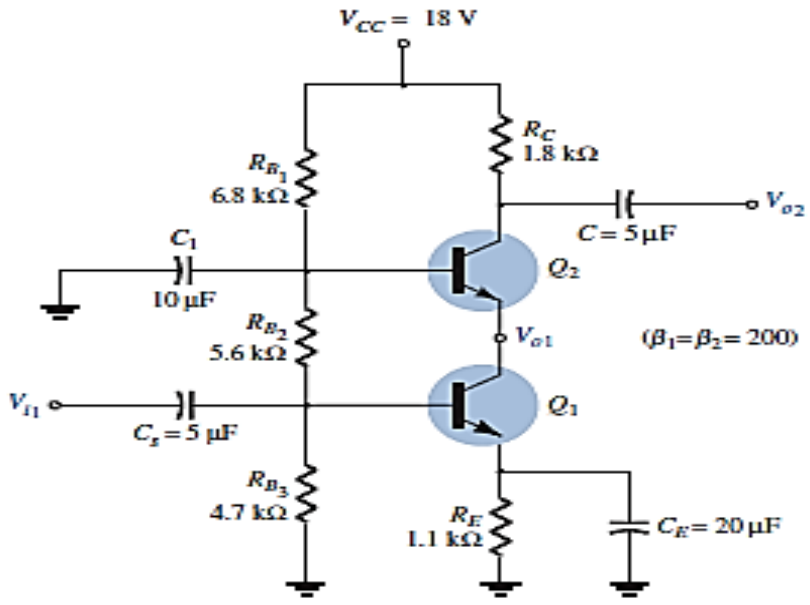

FIG. 71
Practical cascode circuit for Example 16.

Solution: The dc analysis results in

$$V_{B_1} = 4.9\text{ V}, \quad V_{B_2} = 10.8\text{ V}, \quad I_{C_1} \cong I_{C_2} = 3.8\text{ mA}$$

because $I_{E_1} \cong I_{E_2}$ the dynamic resistance for each transistor is

$$r_e = \frac{26\text{ mV}}{I_E} \cong \frac{26\text{ mV}}{3.8\text{ mA}} = 6.8\ \Omega$$

The loading on the transistor Q_1 is the input impedance of the Q_2 transistor in the CB configuration as shown by r_e in Fig 72.

The result is the replacement of R_C in the basic no-load equation for the gain of the CB configuration, with the input impedance of a CB configuration as follows:

$$A_{v_1} = -\frac{R_C}{r_e} = -\frac{r_e}{r_e} = -1$$

with the voltage gain for the second stage (common base) of

$$A_{v_2} = \frac{R_C}{r_e} = \frac{1.8\text{ k}\Omega}{6.8\ \Omega} = 265$$

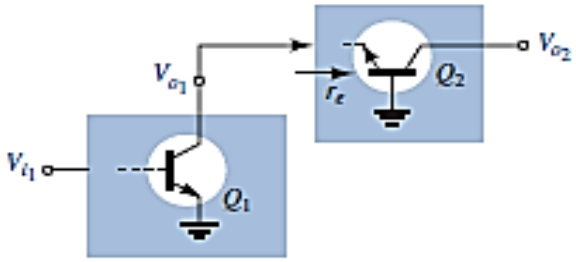

FIG. 72
Defining the load of Q_1.

The overall no-load gain is BJT AC AnAlysis

$AV_T = AV1AV2 = (-1)(265) =$ **-265**

As expected, in Example 16, the CE stage provides a higher input impedance than can be expected from the CB stage. With a voltage gain of about 1 for the first stage, the Miller-effect input capacitance is kept quite low to support a good high-frequency response. A large voltage gain of 265 was provided by the CB stage to give the overall design a good input impedance level with desirable gain levels.