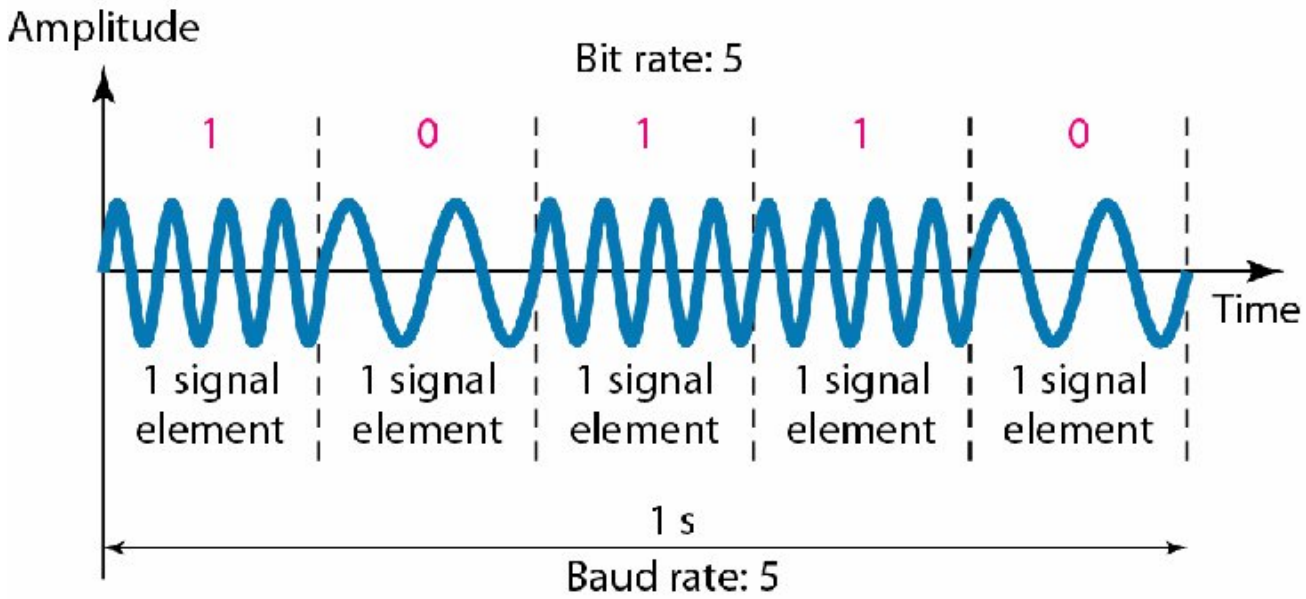
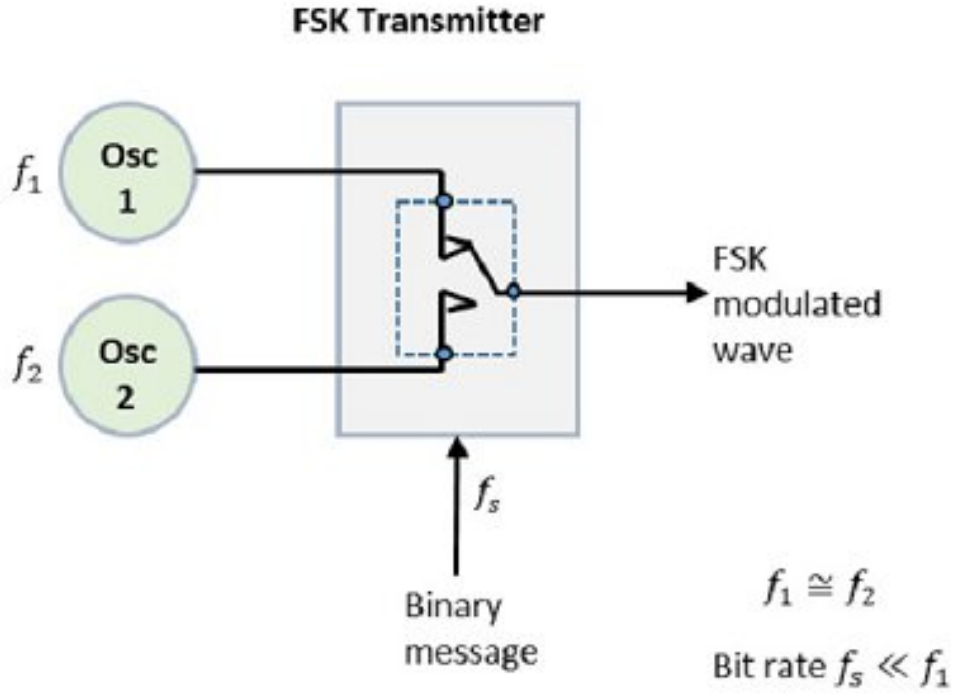
- FSK is the digital modulation technique in which the frequency of the carrier signal varies according to the digital signal changes. FSK is a scheme of frequency modulation.
- The output of a FSK modulated wave is high in frequency for a binary High input and is low in frequency for a binary Low input.

$$s(t) = \begin{cases} A_c \cos(2\pi f_{c1} t) & for\ bit\ \ 1 \\ A_c \cos(2\pi f_{c2} t) & for\ bit\ \ 0 \end{cases}$$



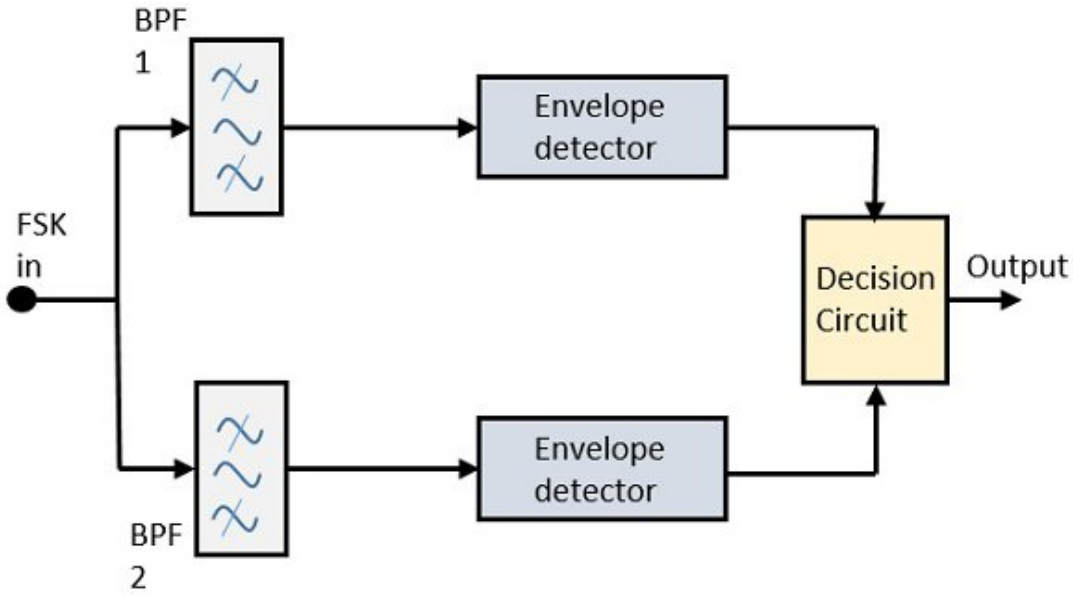
The FSK modulator block diagram comprises of two oscillators with a clock and the input binary sequence. The two oscillators, producing a higher and a lower frequency signals, are connected to a switch along with an internal clock. The binary input sequence is applied to the transmitter so as to choose the frequencies according to the binary input.



The main methods of FSK detection are **asynchronous detector** and **synchronous detector**. The synchronous detector is a coherent one, while asynchronous detector is a non-coherent one.

Asynchronous FSK Detector

The block diagram of Asynchronous FSK detector consists of two band pass filters, two envelope detectors, and a decision circuit as shown in the block diagram below.

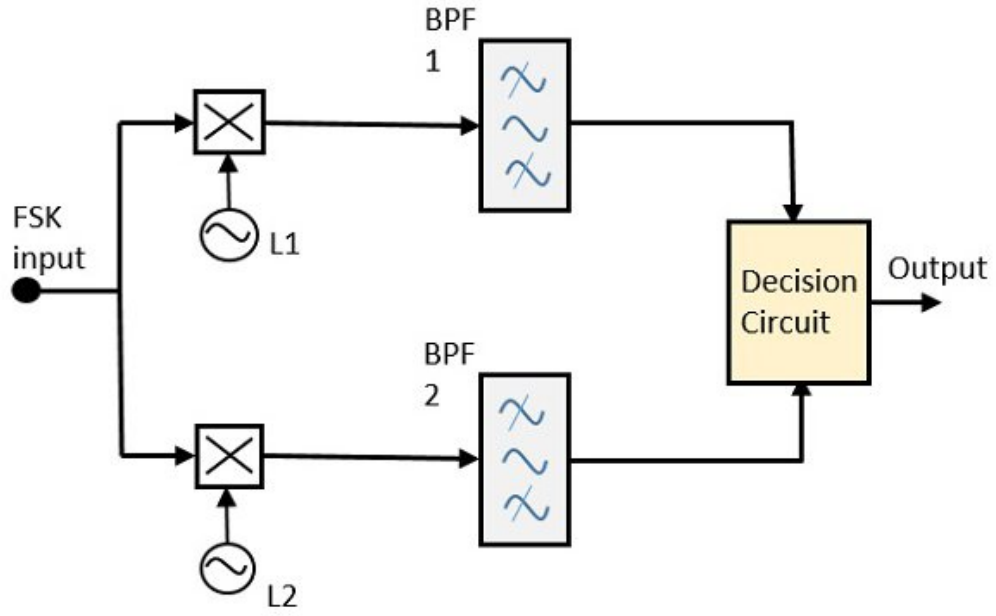


The FSK signal is passed through the two Band Pass Filters (BPFs) tuned to low and high frequencies. The output from these two BPFs look like ASK signal, which is given to the envelope detector. The signal in each envelope detector is modulated asynchronously.

The decision circuit chooses which output is more likely and selects it from any one of the envelope detectors. It also re-shapes the waveform to a rectangular one.

Synchronous FSK Detector

The block diagram of Synchronous FSK detector consists of two mixers with local oscillator circuits, two band pass filters and a decision circuit as shown below:-

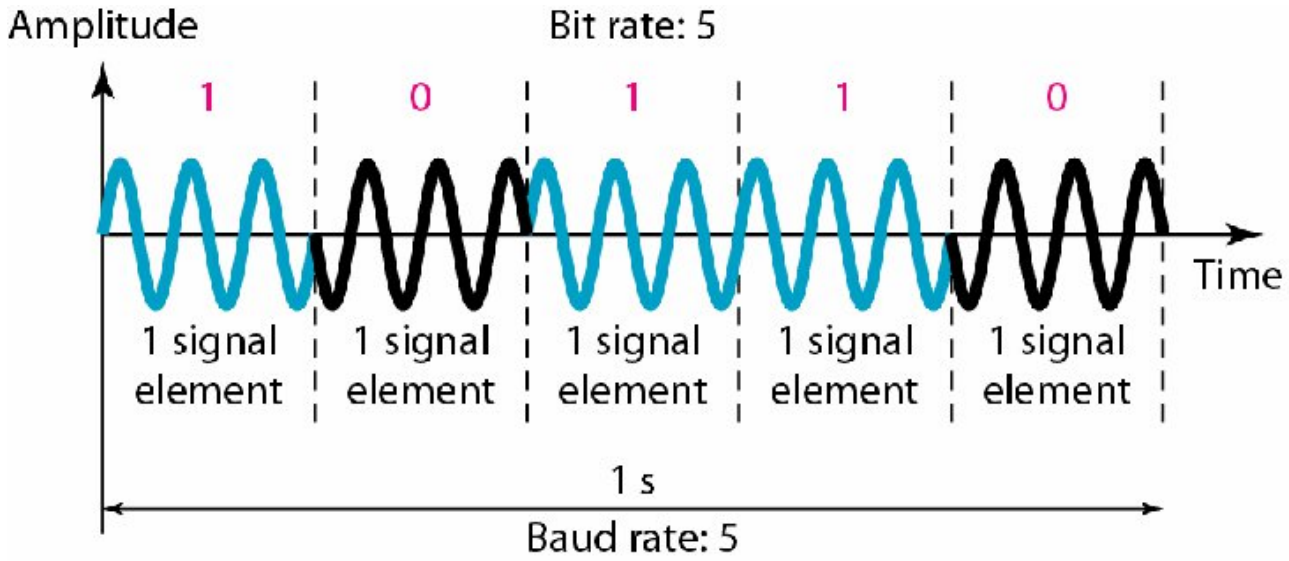


The FSK signal input is given to the two mixers with local oscillator circuits. These two are connected to two band pass filters. These combinations act as demodulators and the decision circuit chooses which output is more likely and selects it from any one of the detectors. The two signals have a minimum frequency separation.

For both of the demodulators, the bandwidth of each of them depends on their bit rate. This synchronous demodulator is a bit complex than asynchronous type demodulators.

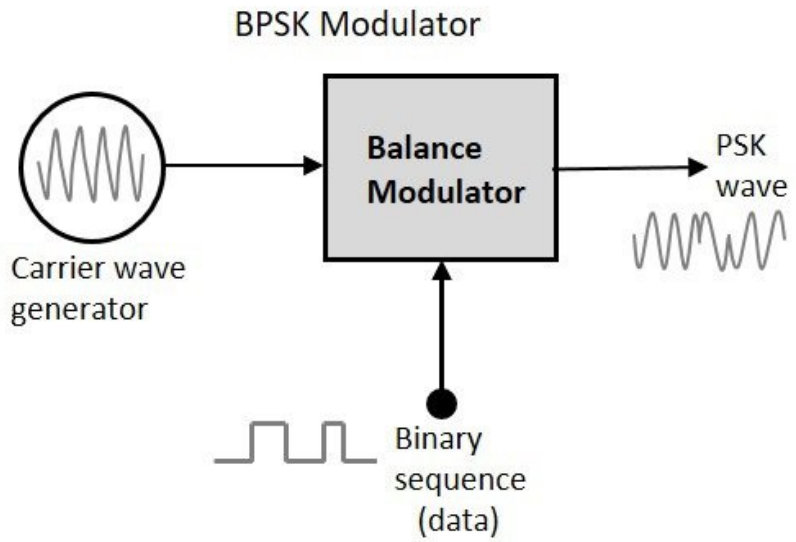
- In PSK, the phase of the carrier is shifted to represent data. Two-Level PSK(Binary PSK) - BPSK uses two phases (0 and 180°) to represent the two binary digits.
  - The resulting transmitted signal for one bit time is:

$$s(t) = m(t)c(t) = \begin{cases} A\cos(2\pi f_c t) \\ A\cos(2\pi f_c t + \pi) \end{cases} = \begin{cases} A\cos(2\pi f_c t) & binary\ 1 \\ -A\cos(2\pi f_c t) & binary\ 0 \end{cases}$$



PSK Modulator

The block diagram of Binary Phase Shift Keying consists of the balance modulator which has the carrier sine wave as one input and the binary sequence as the other input. BPSK is basically a Double Side Band Suppressed Carrier (DSBSC) modulation scheme, for message being the digital information.

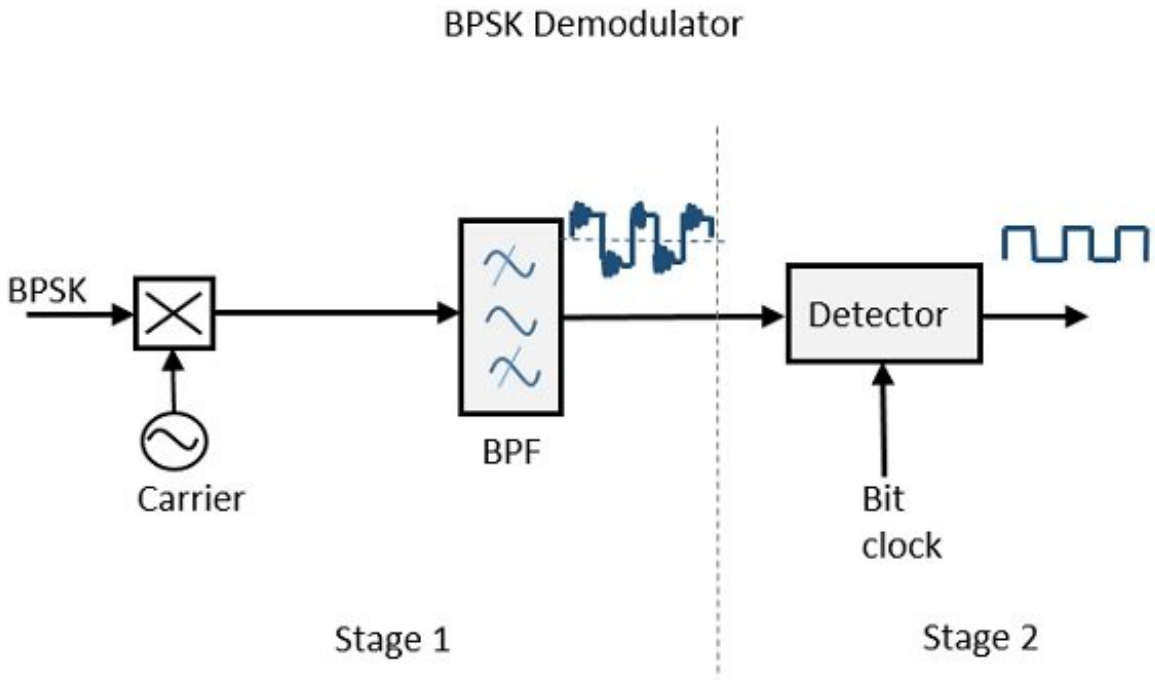


The modulation of BPSK is done using a balance modulator, which multiplies the two signals applied at the input.
For a zero binary input, the phase will be **0°** and for a high input, the phase reversal is of **180°**.

PSK can be expanded to a M-ary scheme, employing multiple phases and amplitudes as different states in which the sine wave carrier takes several phase reversals such as 0°, 90°, 180°, and 270° in case of Quadrature Phase Shift Keying (QPSK).

BPSK Demodulator

The block diagram of BPSK demodulator consists of a mixer with local oscillator circuit, a bandpass filter, a two-input detector circuit. The diagram is as follows.



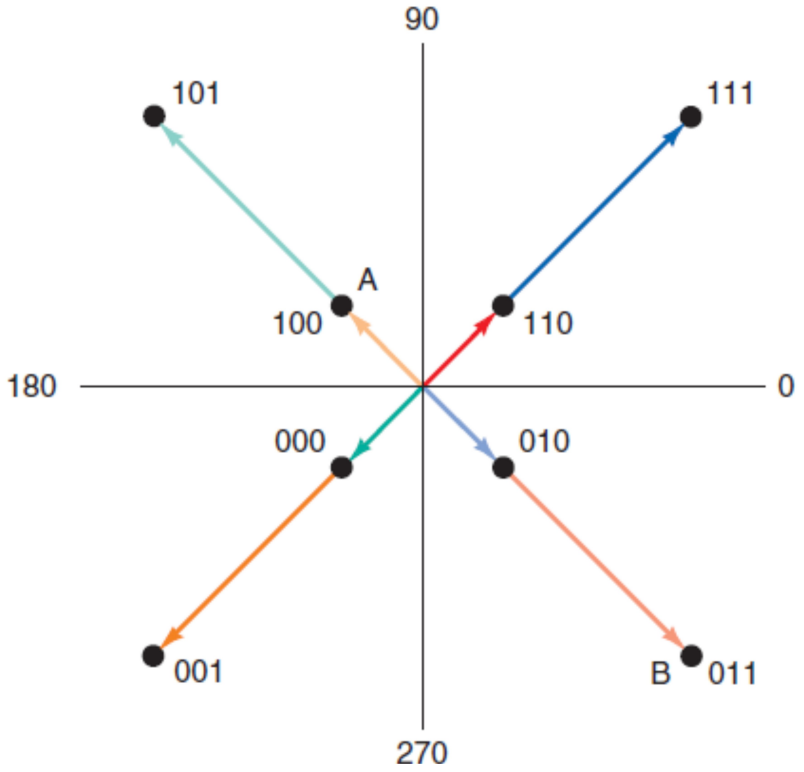
By recovering the band-limited message signal, with the help of the mixer circuit and the band pass filter, the first stage of demodulation gets completed. The base band signal which is band limited is obtained and this signal is used to regenerate the binary message bit stream.

In the next stage of demodulation, the bit clock rate is needed at the detector circuit to produce the original binary message signal.

One of the most popular modulation techniques used in modems for increasing the number of bits per baud is quadrature amplitude modulation (QAM). QAM uses both amplitude and phase modulation of a carrier; not only are different phase shifts produced, but also the amplitude of the carrier is varied

For example, 8QAM uses four carrier phases plus two amplitude levels to transmit 3 bits per symbol as shown in Figure below. The points in the diagram below indicate the eight possible phase amplitude combinations. Note that there are two amplitude levels for each phase position. Point A shows a low carrier amplitude with a phase shift of 135°, it represents 100. Point B shows a higher amplitude and a phase shift of 315°. This sine wave represents 011.

The eight output symbols might be $2\cos(2\pi f_c t + 45°)$, $2\cos(2\pi f_c t + 135°)$, $2\cos(2\pi f_c t + 215°)$, $2\cos(2\pi f_c t + 305°)$, $4\cos(2\pi f_c t + 45°)$, $4\cos(2\pi f_c t + 135°)$, $4\cos(2\pi f_c t + 215°)$, and $4\cos(2\pi f_c t + 305°)$.



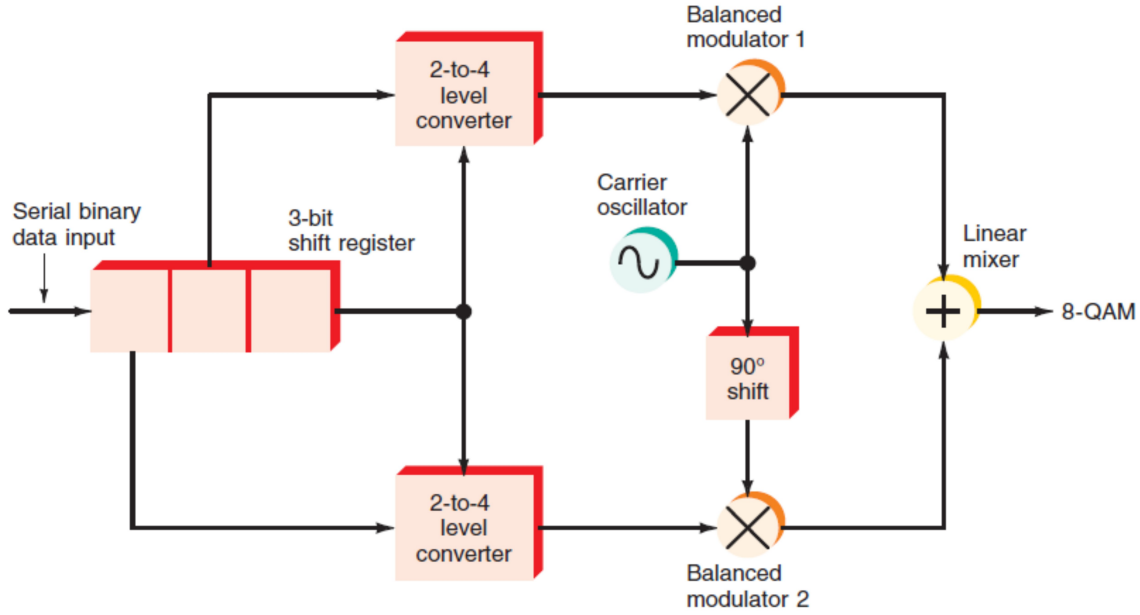
Constellation diagrams for 8-QAM

QAM is similar to ASK modulation except that we put an ASK signal in the in-phase (cosine) and quadrature (sine) modulation term. The mathematical description of this signal is

$$s(t) = a_k \cos(2\pi f_o t) + b_k \sin(2\pi f_o t)$$

where a_k and b_k are multi amplitude values of the form [±1, ±3, ±5, …, ± 2M−1]. For M= 2, there are four terms on the I component and four terms on the Q component.

A block diagram of an 8-QAM modulator is shown in Fig. The binary data to be transmitted is shifted serially into the 3-bit shift register. These bits are applied in pairs to two 2-to-4 level converters. A 2-to-4 level converter circuit, basically a simple D/A converter, translates a pair of binary inputs into one of four possible dc output voltage levels. The idea is to produce four voltage levels corresponding to the different combinations of 2 input bits, i.e., four equally spaced voltage levels. These are applied to the two balanced modulators fed by the carrier oscillator and a 90° phase shifter, as in a QPSK modulator. Each balanced m
amplitude combinations. When these are combined in the line
combinations are produced.



A 16-QAM signal can also be generated by encoding 4 input bits at a time. The result is 12 different phase shifts and 3 amplitude levels, producing a total of 16 different phase-amplitude combinations. Even higher data rates can be achieved with **64-QAM** and **256-QAM**. Multilevel modulation schemes using **1024-QAM to 4096-QAM** are also used. These signals are used in cable TV modems, wireless local area networks (WLANs), satellites, and high-speed fixed broadband wireless applications.

Bandwidth for QAM

The minimum bandwidth required for QAM transmission is the same as that required for ASK and PSK transmission. QAM has the same advantages as PSK over ASK. In 256-QAM, you find that for each symbol you are transmitting (there are 256 symbols), there are 8 bits of information. Assuming the symbol rate remains constant, then for the same bandwidth you are sending 8 times more information when you use 256-QAM than when you use OOK, ASK or BPSK. For 256-QAM, if the bandwidth is 200 kHz, then the bit rate is 8(200,000)/2 = 800 kbps.

Bit Error Rate (BER)

Another factor that clearly impacts the spectral efficiency is the noise in the channel or the signal-to-noise (S/N) ratio. Obviously the greater the noise, the greater the number of bit errors.

The number of errors that occur in a given time is called the **bit error rate (BER)**. The BER is simply the ratio of the number of errors that occur in 1 s of a 1-s interval of data transmission. For example, if 5 errors occur in 1 s in a 10Mbps transmission, the BER is then = 5/10Mbs = 5×10^{-7}